A digital scan converter for weather satellite images

Introduction

All the slow scan image transmission systems have one main disadvantage : the transmission time of a single image is much longer than the time a human eye can memorize it. This simply means that slow scan images can not be viewed on a conventional CRT and some form of storage of the image data is necessary to make it visible for our eyes. Various systems were developed in the past to display such images : special memory CRTs for radar and SSTV and various photo-chemical or electro-chemical systems for faximile images. The principle of operation of a digital memory display device was known, however it was unpractical due to the large memory required to store a single image. Fortunately the cost of digital MOS memories is continuously falling and new, easier to use chips are available on the market. This evolution caused that the digital storage principle has not become only realizable but also the most economical approach for amateurs.

The size of the memory required depends on the geometrical resolution - number of lines of the image displayed and number of the picture elements (pixels) per line and on the radiometrical resolution - number of grey levels of an image. Practical considerations limit the geometrical resolution between 128 pixels × 128 lines (16 k memory) and 512 pixels × 512 lines (256 k memory). Both the limits are imposed by the memory cost : smaller systems (less than 16 k memory) would probably not be much cheaper, larger systems (more than 256k memory) would not produce appreciably better results on conventional TV CRTs although they were much more expensive. On the other hand, the choice of the number of grey levels (the radiometrical resolution) is not straightforward.

Usually 16 grey levels (including black and white) requiring 4 bits of memory per pixel are chosen for low cost systems. Practical experiments have shown that radiometrical resolution is far more important than geometrical resolution in the case of satellite images. Images are still usable with a geometrical resolution of only 64 pixels x 64 lines (less than 1/10 of the original resolution), however, at least 64 grey levels (6 bits of memory per pixel) are required for an IR image to reduce the quantisation effects to tollerable levels.

The scan converter I am going to describe in this article has a resolution of 128 pixels x 128 lines x 64 grey levels yielding a 16k x 6 bit memory. The circuit (see fig. 1) is divided into two functional units built on two separated printed circuit boards. PCB 1 accepts the APT signal (modulated 2400 Hz subcarrier) and transforms it in a digital format suitable to be written in a digital memory. PCB 1 also decodes all the synchronization information of the APT format and it includes the power supply for the whole scan converter. PCB 2 accepts the signals generated by PCB 1, but it can also accept the output of a frame synchronizer to receive HR digital images. PCB 2 includes a line buffer memory (128 x 6 bit), a main frame memory (16k x 6 bit), a TV sync generator, steering circuits for the memories and a D/A converter. The output of PCB 2 is an analog video signal CCIR compatible (320 lines per frame). Adding a suitable RF modulator a conventional TV set (unmodified) could be used as display.

First printed circuit board

The block diagram of the circuits located on the first PCB is displayed on fig. 2. The APT signal is first filtered by a bandpass filter and demodulated. The analog video obtained is

sampled and converted by an 8 bit A/D converter. Only 6 bits are used, which are then converted to a serial format. Synchronization is obtained from the 2400Hz APT subcarrier, all the timing signals are obtained from a PLL synchronized by the 2400Hz subcarrier and followed by a divider chain. Additional circuits provide the initial synchronization (initial phasing) of the image. These circuits recognize synchronization sequences present in the video signal and reset the line frequency divider. In the event these circuits fail because of a poor signal to noise ratio, the image can be manually synchronized.

The power supply delivers all the required supply voltages, positive and negative, from a single positive (negative grounded) +12,6V external supply (not necessarily stabilized). PCB1 includes also an 1MHz clock oscillator, which drives the TV sync generator on PCB 2.

The video demodulator (see fig. 3.) includes a bandpass filter for the APT signal, an AM demodulator and a video low-pass filter. The circuit was designed to accept the APT signal from a tipical FM demodulator (TBA 120 or similar). Since the APT signal contains useful information only between 800Hz and 4000Hz, the S/N ratio can be substantially improved by filtering away out-of-band noise. The FM modulators onboard the spacecrafts do not employ preemphasis and in such a FM system the demodulated S/N ratio deteriorates with the square of the modulation frequency. This means that it is particularly important to filter away noise components above 4kHz and a good low-pass filter, implemented with an operational amplifier, is required. Filtering below 800Hz is less demanding, it is only necessary to efficiently reject the eventual 50Hz mains frequency disturbs and this can sim-

ply be obtained by selecting proper coupling capacitors. The filter is followed by an amplifier which drives the AM demodulator - a full-wave rectifier. Experiments have shown that it is not necessary to have a very good symmetry of the demodulator and a simple inverter is sufficient. The output of the full-wave rectifier is not only the desired video signal but also a very strong component at twice the subcarrier frequency, 4800 Hz. This should not reach the sample and bold circuit and it is filtered away by a low-pass filter. A trimmer is provided to adjust the DC level of the video signal to match the black level of the image with the start of the transfer curve of the A/D converter in order to fully use the available grey scale. A quad op-amp 324 is employed in the circuit of the video demodulator. The supply voltages are filtered by the two 220μ caps and relative resistors.

The 2400 Hz synchronization chain (see fig. 4.) consists of a two stage narrow band 2400 Hz filter and a PLL that supplies the required frequencies to the clock generator (fig. 5.). CMOS inverters are used as active components in the 2400 Hz filter because they have a smooth and well defined symmetrical limiting characteristic. This is not true for conventional operational amplifiers, which are subjected to saturation, ringing, unsymmetrical limiting and similar problems when operated with high level signals. The circuit shown in Fig. 4. allows wide tolerances of both active and passive components of the filter and the high input impedance of the CMOS inverters allows a wide choice of R and C values. It is only important to use CMOS gates of the A or UB series, the B series CMOS gates have a too high uncompensated gain and usually oscillate in feedback circuits.

The output of the filter is capacitively coupled to the self-bia

sing input of the 4046 PLL circuit. Phase comparator I (exclusive-or gate) is used since some input pulses might be missing because of noise and/or very deep modulation of the 2400Hz subcarrier. The VCO oscillates nominally at 38.4 kHz, 16 times the subcarrier reference. R2 (68k connected to pin 12) is not functionally necessary, it only ensures the start of the VCO under any power-up conditions. Wide tolerances are allowed for the 4046 VCO section, therefore it might prove necessary to modify the value of the VCO capacitor (1nF).

The VCO frequency is divided by 16 by the 4024 binary counter. 19.2kHz, 9.6 kHz, 4.8kHz and 2.4kHz are obtained at the outputs of the 4024. These frequencies drive the clock generator (fig. 5.), divided by 8 they give the pixel sampling frequency.

The choice of the sampling frequency is not trivial and several factors have to be considered. The data rate of an APT format is about 3200 words per second. Since this is limited by the transmission channel bandwidth, it is of little use to have a higher sampling frequency. The sampling frequency must also be adapted to the size and format of the frame memory available. As the available memory (128x 128 pixels) is much smaller than the APT image format (800 x 800 pixels), it should be possible to display the complete image at reduced resolution or various "magnifications" of sectors of the image at less reduced or even original geometrical resolution. This is possible by changing the pixel sampling frequency.

In theory there is no relationship between the sampling frequency and the APT subcarrier frequency. In practice the remainder subcarrier frequency or its harmonics have to be care-

fully filtered away from the video signal. If these components reach the sample and hold stage, the beating with the sampling frequency (or its harmonics) will be visible as vertical bars on the image (diagonal bars if the two frequencies are not in a constant phase relationship). In the case of a 16k (128 x 128) memory it is possible to choose 2400Hz or its submultiples as sampling frequencies. As in this case no beating products (except a DC component) will be produced below the sampling frequency, much less filtering of the video signal will be required. However, it is important that the sampling frequency is phase locked to the subcarrier frequency in this case. Phase locking of the sampling frequency to the subcarrier frequency brings other advantages: it provides an excellent tracking of tape speed variations in the case of recorded images.

Table 1 shows the possible display formats by selecting these sampling frequencies: 2400Hz, 1200Hz, 600Hz and 300Hz.

A CMOS transmission gate (4007) is the sampling switch. (fig. 5.). The input impedance of the A/D converter ADC 0804 (National Semiconductor) is sufficiently high so that no additional amplifier is required for the holding function (100n cap). The 680Ω resistor from pin 9 (V_{ref}) to ground defines the dynamic range of the A/D converter from 0V to about 2V. The ADC 0804 has an internal clock oscillator (schmitt-trigger gate), the external components are a resistor and a capacitor connected to pins 4 and 19. A clock frequency of 800kHz gives a conversion time of about 100μs. The conversion is started at the leading edge of the conversion command signal (see fig. 9.). When the conversion is completed, the data is transferred to the output latch of the ADC 0804. An 8 input NAND gate detects the overrange, which is displayed by a LED. This

indicator is very useful to adjust correctly the signal level at the input of the video demodulator. The relative potentiometer is adjusted correctly when the LED just starts flickering indicating that the dynamic range of the A/D converter is fully utilized without excessive clipping.

The parallel data at the outputs of the ADC 0804 are serialized by the multiplexer 4051 which is driven by the divider 4024. The clock generator includes also a decoder logic to generate the conversion command and the pixel clock. All the PCB 1 output signals : the serial data, the coherent bit clock, the pixel clock (fig. 5) and the line clock (fig. 7.) are buffered by tri-state gates (4503 or 40097). The $\overline{\text{enable}}$ input (fig. 5) is usually connected to GND. When it is tied to +5V it disables the tri-state buffers so that signals from another source (for example from the frame synchronizer as in fig. 1.) can be fed to PCB 2.

The line sampling clock is derived from the pixel sampling clock. Here it is important to notice that the line sampling clock equals the image line frequency only when the maximum geometrical resolution is to be retained. When an image is to be displayed at reduced resolution it is not only necessary to reduce the pixel sampling clock to lower the horizontal resolution but it is also necessary to reduce the line sampling clock to lower the vertical resolution to avoid a severe geometrical distortion. For example, if the image is to be displayed at 1/4 of the original resolution (nearly the whole image in the case of a 128 x 128 memory), then the pixel sampling rate should be lowered to 1/4 of the maximum sampling rate and only every fourth line of the image should be written into the memory. This means that the ratio between the pixel sampling frequency and line sampling frequency remains constant for a fixed

image format and memory size. In the case of a 128×128 memory displayed on a TV screen with a 4:3 aspect ratio the ratio between the two sampling frequencies is 600 for Meteosat and both Meteor VIS standards and 1200 for the Noaa standard.

A half and a quarter of the pixel sampling frequency are available respectively at the outputs Q4 and Q5 of the 4024 divider on fig. 5. A further division by 300 is performed by the line clock divider (fig. 7.) yielding the required ratios (600 or 1200) between the two sampling frequencies. Aux outputs are provided for other satellite standards, for example for the (very seldom active) Meteor IR, which requires a ratio of 150 between the two sampling frequencies.

The initial synchronization logic (fig. 6.) can work automatically by decoding the start and stop tones of Meteosat wefax transmissions or manually by decoding the tone sync pulses of Meteosat, Noaa and Meteor. Three LM567 PLL tone decoders are tuned to 300Hz, 450Hz and 840Hz. Since very high capacitance values would be required at the output filter terminal (1) of the first two LM567, external delay gates are connected to their outputs(8) The 300Hz and 450Hz decoders control a SR flip-flop to implement the automatical start-stop function. A delayed 300Hz pulse connects the MSB of the A/D converter to the $\overline{\text{reset}}$ of the line clock divider. The synchronization pulses, which immediately follow the 300Hz start tone, in this way synchronize the line divider automatically.

The LM567 is a narrow band tone decoder and it is not very suitable to detect very short tone bursts, like the horizontal sync pulses of the Noaa and Meteosat images (7 cycles). The operation of the 840Hz detector is not very reliable since it is also sensitive to image patterns similar to sync pulses and

noise and sometimes it is necessary to repeat the manual sync operation. On the other hand, Meteor spacecrafts (120 lines/min) have much longer tone sync pulses (16 cycles), unfortunately the frequency of these bursts is not exactly 300Hz and a separate tone decoder would be required for best results.

However, when receiving polar orbiting satellites, the S/N ratio is usually very poor at the beginning of the acquisition, especially when using an omnidirectional antenna, sync pulses are unusable and a completely manual synchronization has to be performed.

The line clock divider (fig.7.) is made of two dividers. The first is a divider by 3 and it is followed by a divider by 100. The divider by 3 (4027 and two NAND gates) can also be preset to divide by 2 or by 4 by two pushbuttons. In this way a slightly higher or lower line clock frequency can be generated to manually "shift" the image in both directions. The shift is naturally proportional to the time the pushbuttons have been depressed. A 4518 works as a divider by 100. The diodes at the outputs of the 4518 are connected as an AND gate to narrow the output pulse. This is necessary for some transmission standards, for example to receive the Meteor IR images (20 lines/minute).

The first printed circuit board includes also the power supply (fig.8.) for both the printed circuit boards. The required external supply is nominally 12,6V, however the scan converter can operate between 10V and 15.5V at room temperature. The nominal current consumption is between 400 and 450mA. The diode 1N4007 should protect the circuits from a polarity inversion and the choke VK200 precludes the disturbs generated by digital circuits from reaching the receiver via the supply connections. A 7805 three-terminal voltage regulator (TO-220 case)

delivers the +5V supply. The voltage regulator IC should be mounted on a suitable heatsink (wall of the box). No insulation hardware is needed since the tab of the 7805 is connected to ground. A 555 is connected as a multivibrator. Its output is rectified to obtain a negative supply voltage of about -8V. The -5V supply is obtained by a simple zener + transistor regulator.

PCB 1 includes also an 1MHz LC oscillator to obtain the TV line and field frequencies on PCB 2. Since the format of the TV signal generated by PCB 2 is not exactly CCIR(320 lines instead of 312.5 lines per field), a variable oscillator is preferred to a crystal one. Practical experiments have shown that some TV monitors (or modified TV sets) are more sensitive to the line frequency (loss of horizontal sync) while other are more sensitive to the field frequency (interference with the 50Hz mains!)

The first PCB has the dimensions of 85mm × 190mm and is single coated (see fig. 11.). The location of the components, the connections and jumpers are displayed on fig. 10. The connections with the switches, pushbuttons, potentiometer, connectors and the second PCB are numbered from 1 to 30 (the numbers in the circles). As there is little space on PCB 1, the resistors should be mounted vertically.

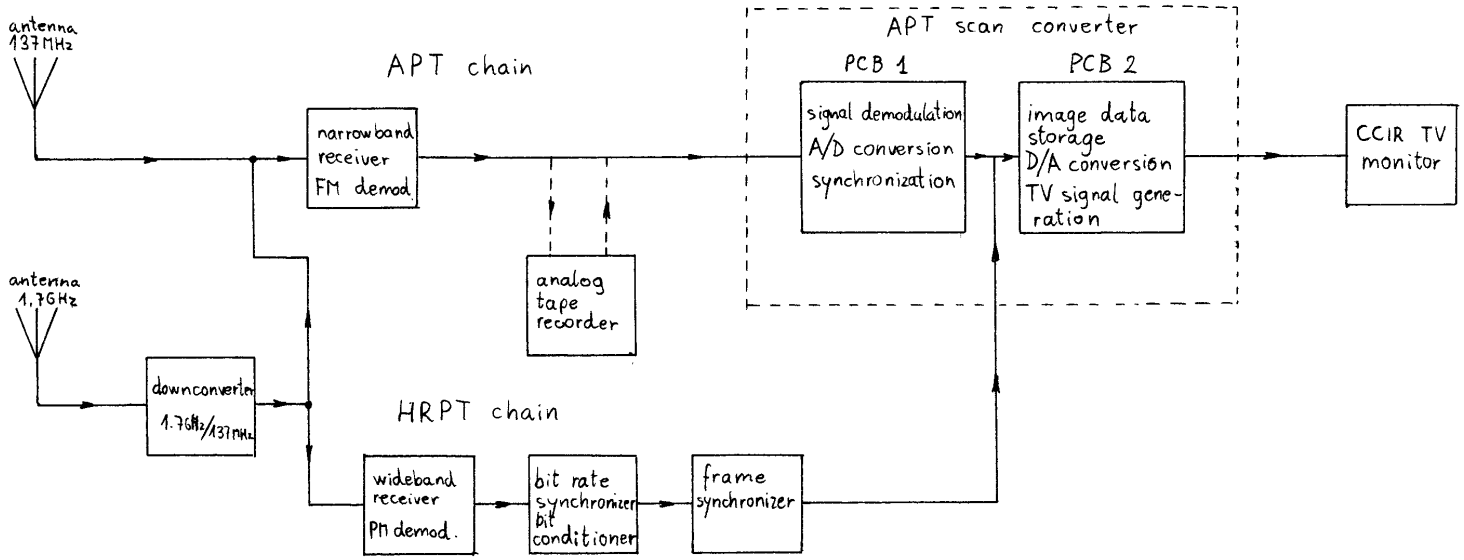

Fig. 1. - Block diagram of an APT/HRPT receiving station.

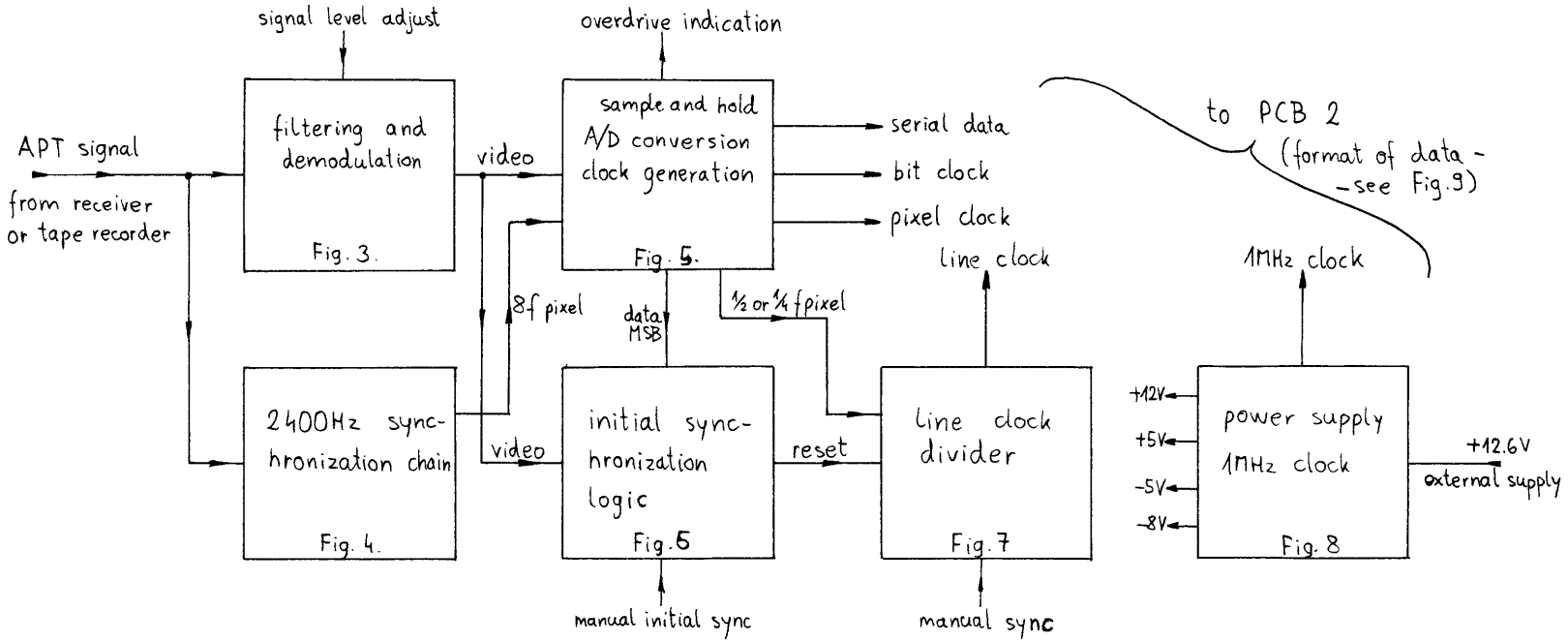

Fig. 2. – Block diagram of PCB 1.

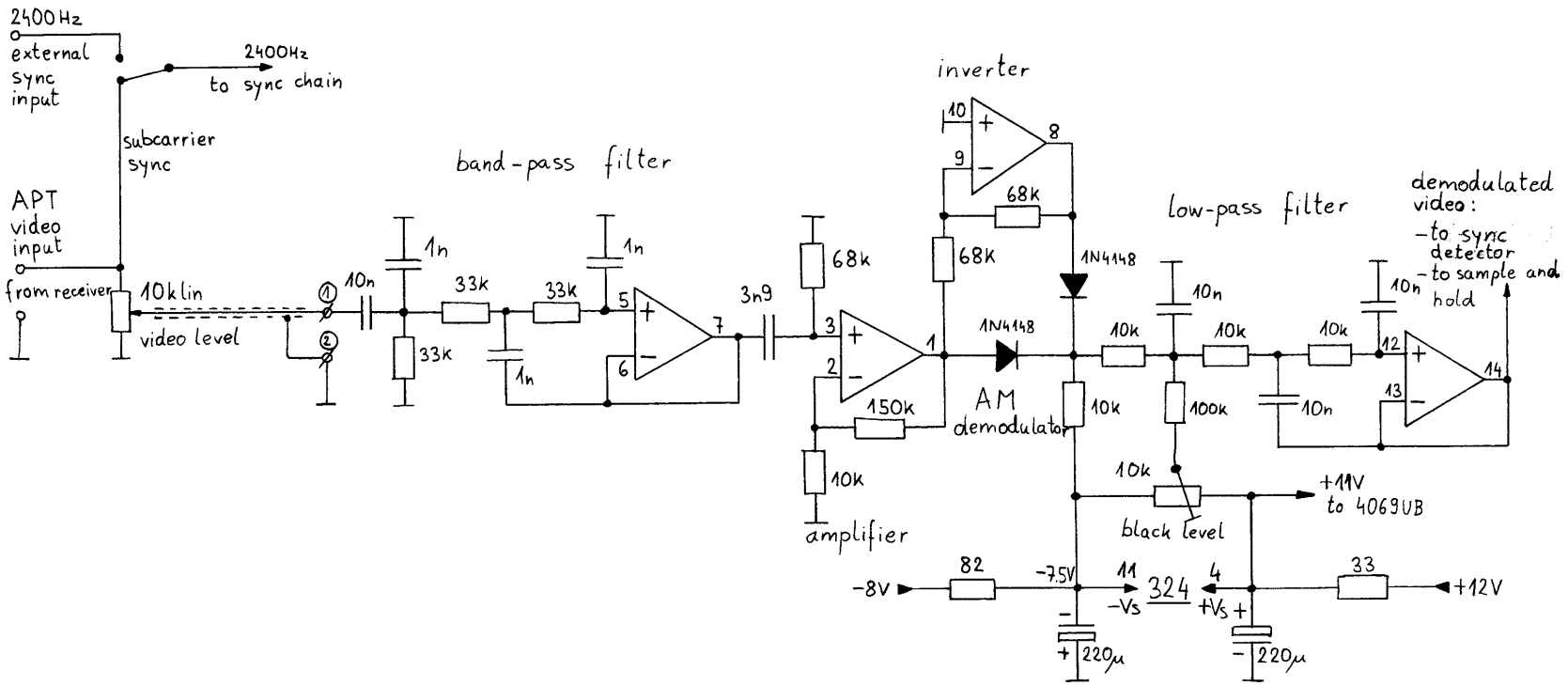

Fig. 3 - Video demodulator.

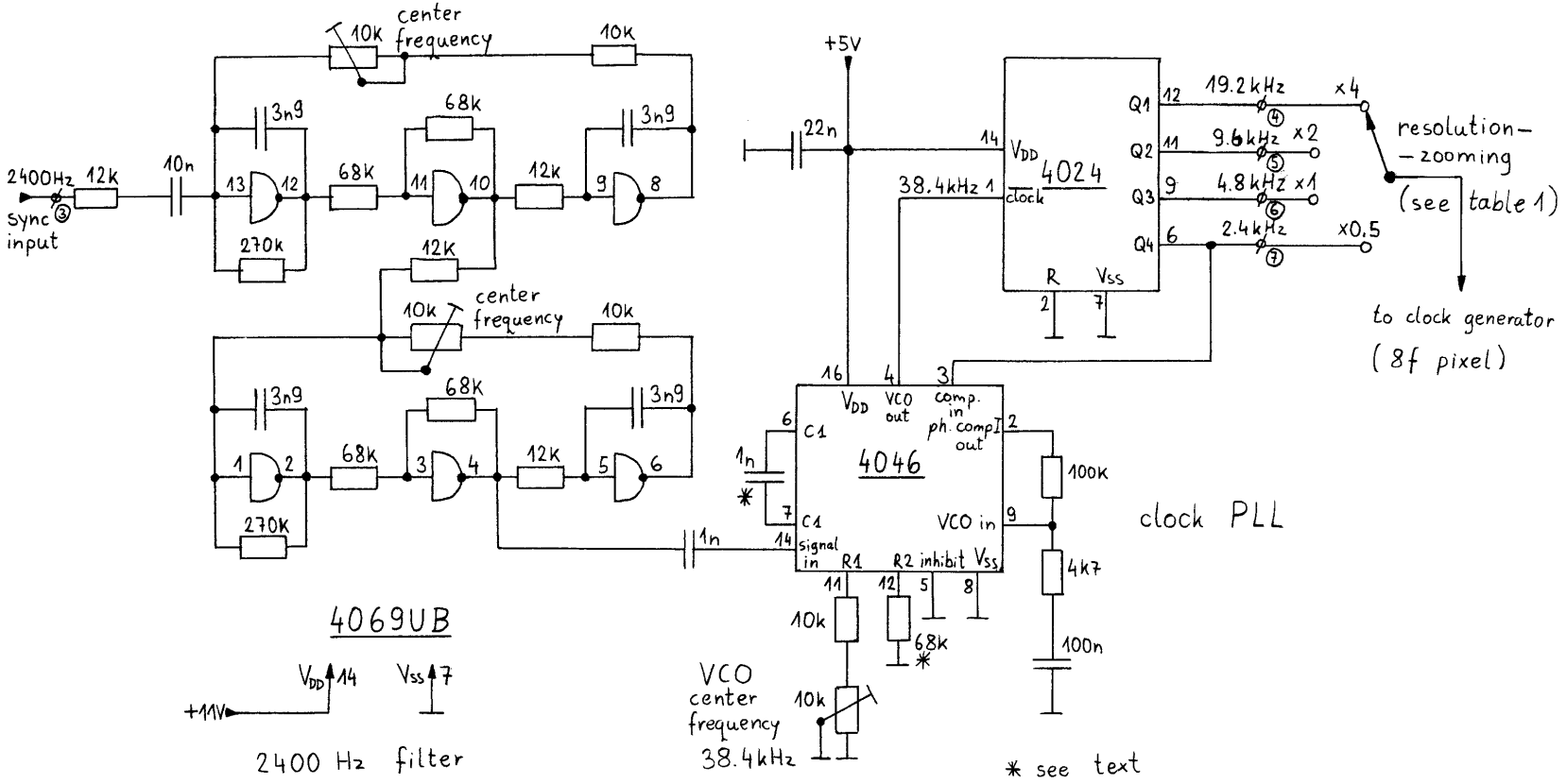

Fig. 4 - 2400 Hz synchronization chain.

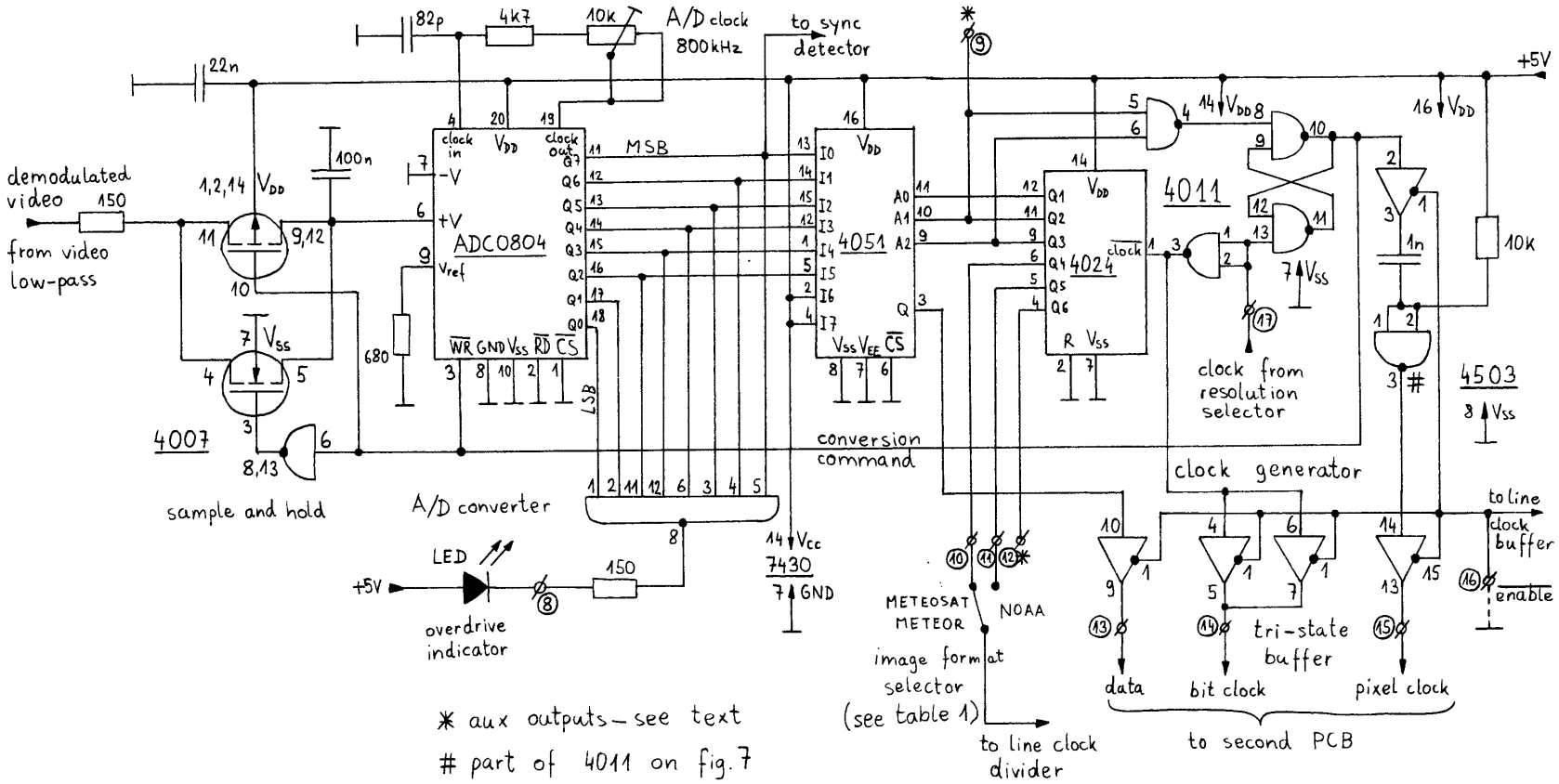

Fig. 5 – A/D converter and clock generator.

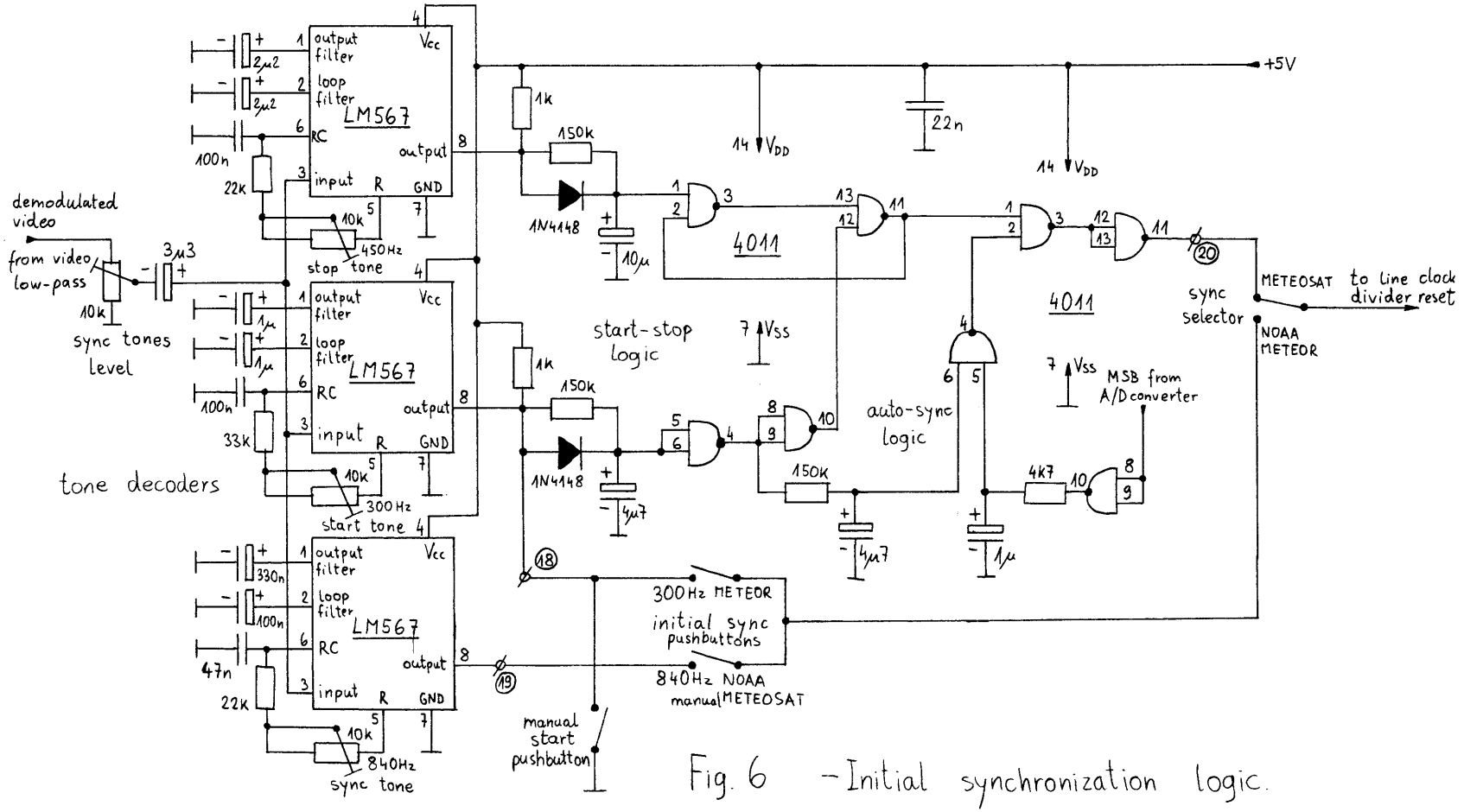

Fig. 6 - Initial synchronization logic.

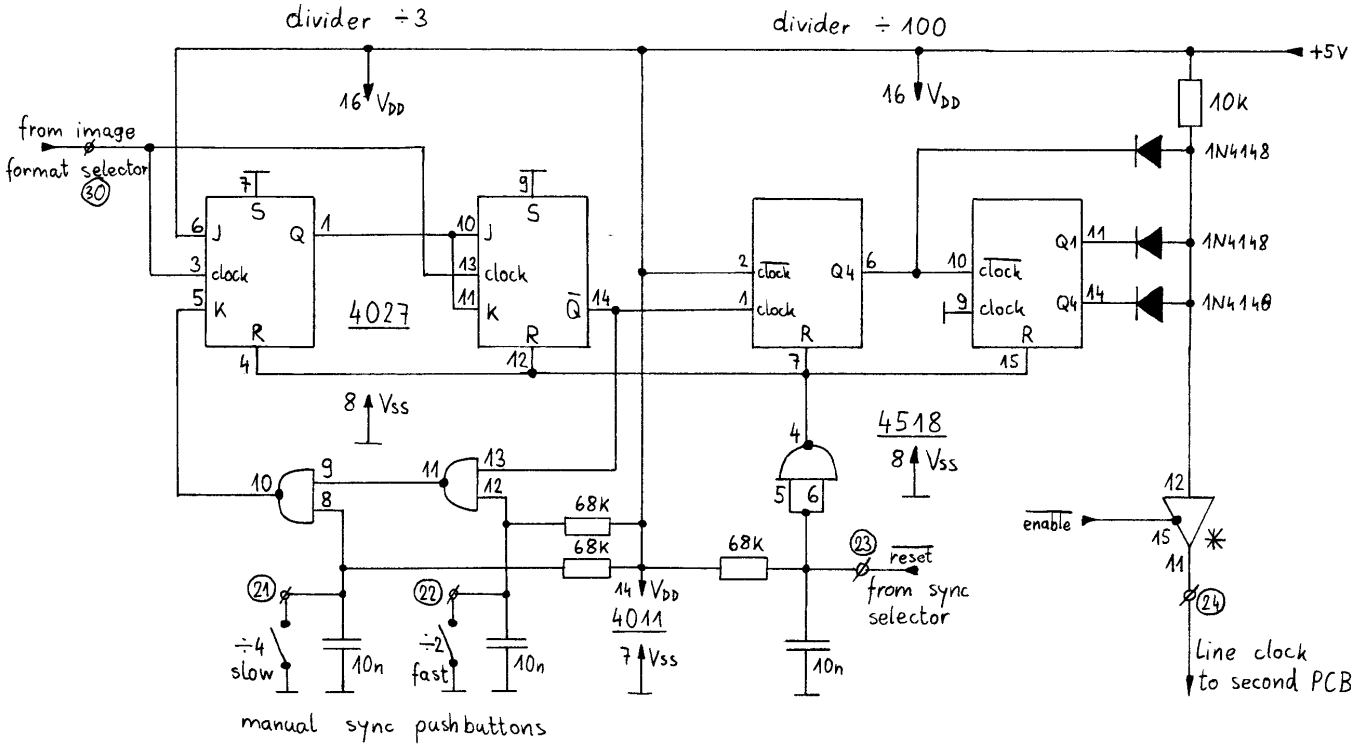

Fig. 7 — Line clock divider.

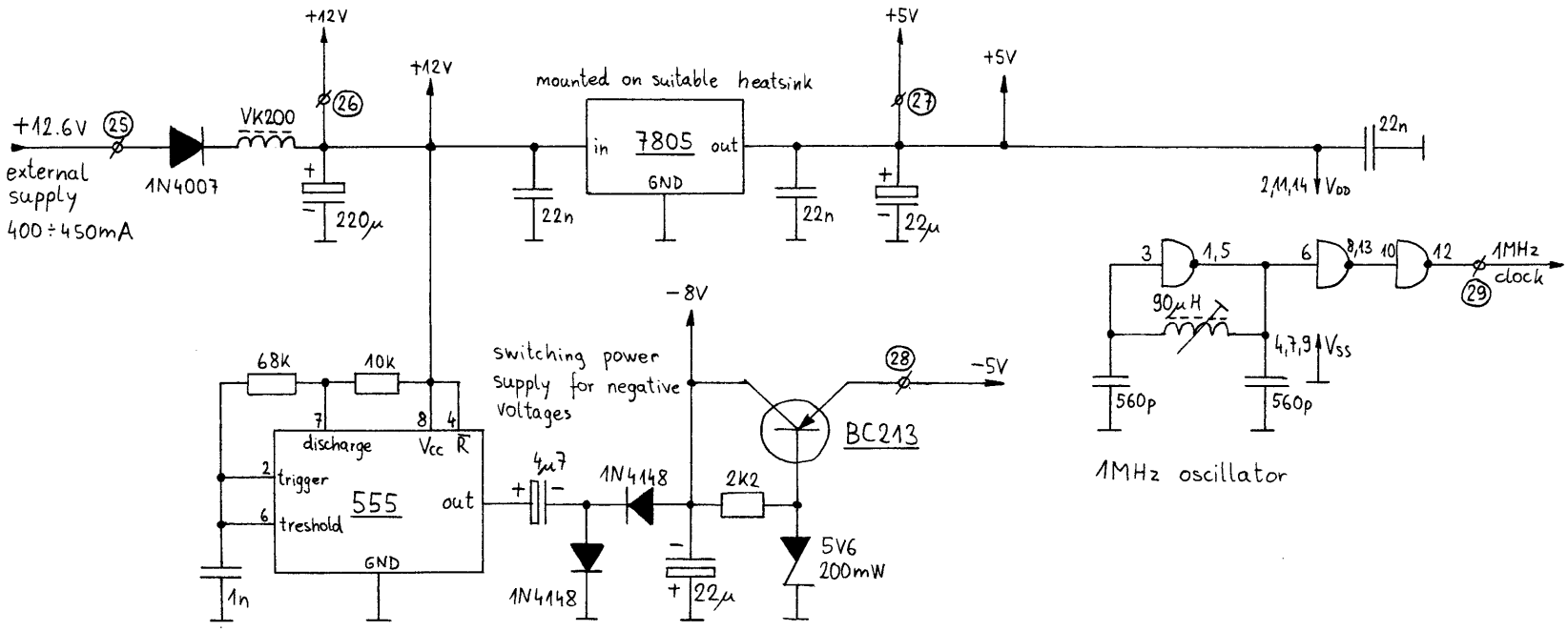

Fig. 8 – Power supply and 1MHz clock oscillator.

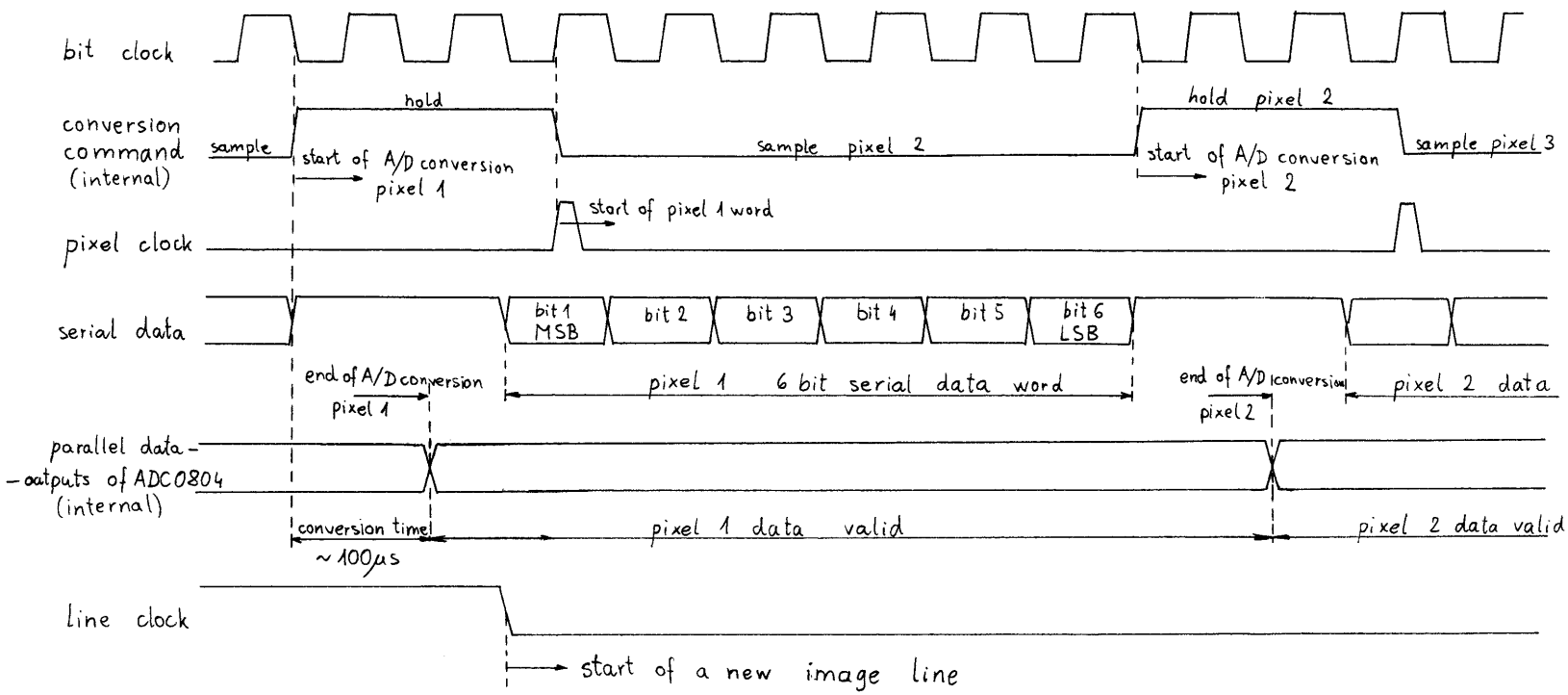

Fig. 9. – Output data format as generated by PCB 1.

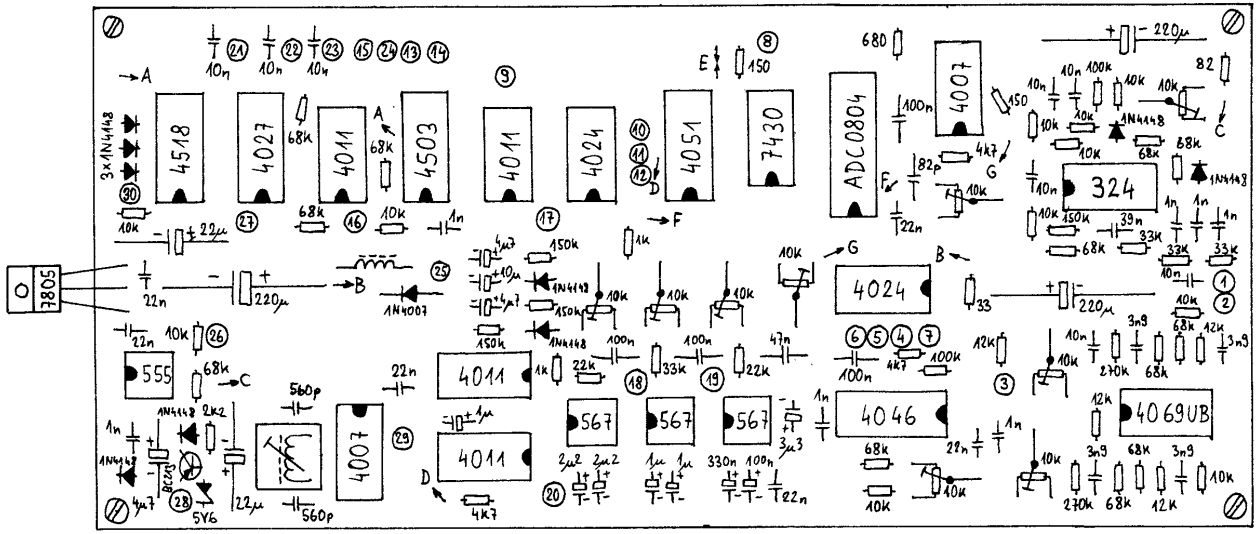

Fig. 10 - Location of the components on PCB 1.

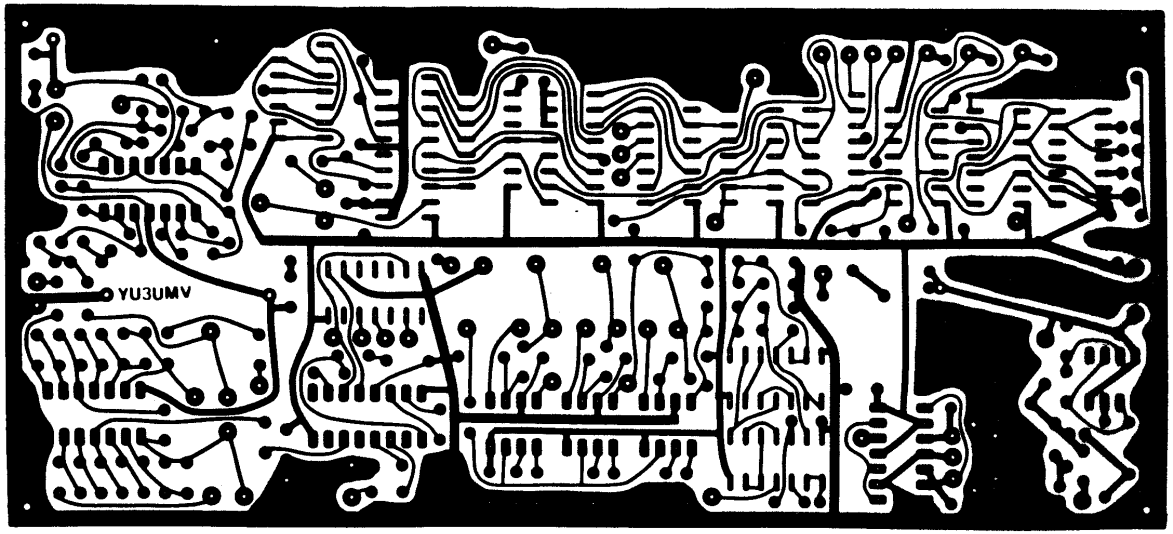

Fig: 11 - First PCB , single coated , copper side.

	received spacecraft:	Meteosat APT 240 lines/min	NOAA APT 120 lines/min	Meteor 240 lines/min	Meteor * 120 lines/min
	image format selector	Meteosat-Meteor	NOAA	Meteosat-Meteor	Meteosat-Meteor
resolution-zooming selector	x 4	x 4	x 4	x 4	
	x 2	x 2	x 2	x 2	x 4
	x 1	x 1	x 1	x 1	x 2
	x 0.5		VIS + IR		x 1

*external 2400 Hz sync required

Table 1 - Image formats that can be displayed. (16k memory)

Second printed circuit board

The block diagram of the circuits located on the second PCB is displayed on fig. 12. PCB 2 accepts the signals generated by PCB 1 (serial data with coherent clocks) or the output of an external frame synchronizer in the case of high resolution digital image reception. The incoming data is written in a line buffer memory first. When the buffer memory is full, containing all the data of an image line, its content is copied into the main frame memory.

The frame memory is continuously scanned to obtain a continuous TV signal at the output of PCB 2. A clock generator, driven by the 1MHz oscillator on PCB 1, delivers all the necessary clocks and addresses to scan the frame memory as well as TV sync and blanking pulses to complete the generated TV signal. All the signals are combined in the D/A converter which delivers a standard analogue video signal of negative polarity. The D/A converter is followed by a sample and hold stage to suppress the D/A switching transients and thus improve the picture quality.

The line buffer memory and associated control logic are displayed on fig. 13. This circuit has two operating modes. In the first mode, the buffer memory accepts the input data in serial format and the control logic (bit counter and pixel counter) is clocked by the input signals (bit clock and pixel clock). As soon as the buffer memory is full, the logic enters into the second mode. During the first next TV vertical flyback period the data from the buffer memory are rewritten into the frame memory. In the second mode, the logic is controlled by clocks generated by the TV sync generator. As soon as the duplication into the main memory is completed, the logic is ready to receive a new line clock pulse, which brings

it back into the first operating mode.

Data is written into the buffer memory in serial format, the serial to parallel conversion takes place during the rewriting into the frame memory. The dual D flip-flop 74LS109 synchronizes the serial data at the input and output of the 2102A line buffer memory. In the first mode, the bit counter 4029 advances on each bit clock pulse modifying the address of the 2102 A memory. The bit counter stops when it reaches the state "8" and eventual further data are ignored. The pixel clock resets the bit counter and thus enables a new pixel to be written into the buffer memory. The pixel clock also advances (or defeats) the pixel counter. After 128 pixel clock periods the buffer memory is full. The Q4 output of the second 4029 of the pixel counter goes to a logic high state, blocking the pixel counter and switching the logic into the second operating mode. This transition is also memorized by the first synchronization flip-flop (first half of the 4027). The second synchronization flip-flop is triggered by the TV vertical blanking pulse (clock 3 = = 48.8 Hz) to copy the information from the first sync FF. The line copy cycle last 6 TV lines (see fig. 21). Here it is important to notice that the 2102A line buffer memory is scanned in a different way than during writing. During each TV line one bit of each pixel (128 pixels in total = 1 line), starting from the MSB, is copied into the corresponding frame memory chip 4116. In this way also a serial to parallel conversion is performed. The 4029 bit counter is clocked by the TV line frequency (clock 2 = 15.6 kHz) during the copy mode and the address multiplexer (2 × 74LS157) switches the pixel addresses of the 2102A line buffer memory in parallel with the frame memory pixel addresses (HA0 to HA6).

A line clock pulse resets the pixel counter (2 × 4029) ena-

bling the logic to write a new line into the buffer memory. The pixel counter can be preset to two different values (0 or 127) by the scan selector. If the image to be displayed was scanned in the W→E direction, the pixel counter should be reset to 0 and should count up. On the contrary, if an E→W scanned image is received, the two 4029 should be preset to 127 and should count down to write the information in the right order into the 2102A line buffer memory and preserve the correct geometrical orientation of the image to be displayed.

The TV sync and main frame memory scan generator is depicted on fig.14. and 15. The TV sync generator is simply a divider chain that triggers some monostables to obtain the various pulses. Since the 312.5 lines per field of the CCIR standard are not easy to obtain, a field of 320 lines was selected. If the line frequency (15625 Hz) is assumed to be correct (and TV monitors are usually very sensitive to the line frequency), then a field frequency of 48.8Hz instead of 50Hz is obtained. This slight difference is usually tolerated by TV monitors. However, in some cases it is preferable to have an exact field frequency since the beating with the 50Hz mains frequency may result very disturbing with some low quality TV monitors (modified commercial TV sets). The solution is to retune the 1MHz clock oscillator (PCB 1) and, if necessary, the horizontal oscillator of the TV monitor.

The monostables to obtain the sync pulses are built with the 4011 gates. Another monostable generates the delay from the horizontal sync pulse to the edge of the useful image. Varying this delay it is possible to adjust the horizontal position of the image displayed on the TV monitor. This monostable starts the horizontal scan oscillator (2.5MHz when active), built with the two monostables of the first 74LS123. Each period of the hori-

zontal scan oscillator equals the time of one TV pixel (fig. 18). These periods are counted by the pixel counter (2 × 74LS161) generating the horizontal (row) addresses to scan the frame memory. When 128 pixels have been counted, the pixel counter blocks the horizontal scan oscillator, which is then started again in the next TV line by the next line pulse.

The 4116 dynamic memories require two clocks named $\overline{RAS}$ and $\overline{CAS}$. Since the memory access cycles correspond to the pixels to be generated, the $\overline{RAS}$ clock is simply generated by the horizontal scan oscillator. The second 74LS 123 generates the delayed $\overline{CAS}$ # clock which switches the the address multiplexer (fig. 15.). The $\overline{CAS}$ clock is also generated by the multiplexer and it is only a slightly delayed $\overline{CAS}$ # clock.

The TTL LS circuits are not able to drive high capacitance reactive loads and pull-up resistors are required on the $\overline{RAS}$ and $\overline{CAS}$ lines, although the 4116 memories are specified fully TTL compatible.

The TV pixel width (and hence the useful picture width = 128 pixels) can be adjusted continuously by changing the horizontal scan oscillator period with the relative trimmer. On the other hand, the pixel height can hardly be adjusted, since a pixel can only be an integer number of TV lines high. Since the frame memory has 128 lines and the TV picture has 250 ÷ 280 useful lines, a logical choice is to have the pixels two lines high yielding 256 useful lines. This is the reason why the line counter (2 × 4029 on fig. 15.) is driven by half the TV line frequency (clock 4 = 7.8 kHz). In this way every image line is read out twice consecutively to generate two identical TV lines.

There are several ways how to introduce new information

into the frame memory, possibly without destroying the previous information. Scrolling is probably the most elegant method, since it continuously provides a useful display acting like a window moving along the image. Although possible, it is not very smart to copy nearly all the information stored in the frame memory one line up or down, it is much easier to modify the vertical (column) addresses to implement the scroll function. In practice it is only necessary to increment the starting address of the line counter. During the vertical flyback period the line counter is held preset by the content of the scroll counter. A new line of image data will hence appear as the first line at the top of the image. If a scroll-down is desired, the scroll counter should be incremented <u>before</u> a new line is copied into the frame memory and the line counter should count down. On the other hand, if a scroll-up is desired, the scroll counter should be incremented <u>after</u> a new line has been copied into the frame memory and the line counter should count up. This can be acheived by simultaneously changing the polarity of the scroll clock by an exclusive-or gate and the up/<u>down</u> control (pins 10) of the 4029s of the line counter.

There are four possible combinations of image scanning, however only two of them: N → S, W → E and S → N, E → W are usually used by weather satellites. As a consequence, only the combinations scroll up, scan right and scroll down, scan left are valid and the scan selector (fig. 13.) and the scroll selector (fig. 15.) can be replaced by a single switch.

The main frame memory is made of six 16 kbit 4116 dynamic RAM memories (see fig. 16.). Each 4116 chip stores one bit of each pixel of the image. Data is written sequentially into the memories (see also the description of the copy cycle)

and separate write commands $\overline{WR0}$ to $\overline{WR5}$ are provided. The output of the frame memory is a 6 bit parallel word (D0 to D5), which is passed to the D/A converter. The dynamic memories require a complete refresh every 2ms by accessing all possible row addresses. In this circuit all the row addresses are accessed during every TV line (64µs) and thus automatically refreshed. The 4116 memories need 3 supply voltages: $V_{BB} = -5V$, $V_{CC} = +5V$ and $V_{DD} = +12V$. Only the V_{DD} supply has a significant current drain, however both V_{DD} and V_{BB} supplies require very good bypass due to the very strong AC components.

The D/A converter is shown on fig. 17. Since the data at the output of the frame memory is only valid for a fraction of the read cycle, a 6 bit latch 74LS174 is used to extend the validity of the data through the whole cycle (fig. 18.) The MC1408 is a current multiplying 8 bit D/A converter. The output current at pin 4 is a fraction of the reference current flowing into pin 14. TV sync pulses are fed to the MSB (D7) of the D/A converter, image data is fed to the following six inputs D6 to D1 and the LSB (D0) is not used. In this way sync pulses are larger (50% of the composite video signal) than prescribed by the TV standard. The blanking signal is fed to the reset of the data latch to force the outputs to zero during the blanking period.

The switching transients (output settling time) of the MC1408 amount to about 100ns. A transconductance amplifier LM3080 samples the waveform at the output of the MC1408. The sampling amplifier is switched on and off by the 2.5MHz sampling clock. The 4k7 trimmer is to be adjusted as a compromise between slew rate and 2.5MHz sampling clock leakage. The hold amplifier is simply a source follower. Since the 2N3819 fet works in the proximity of $V_{GS} = 0$, it is recomended to use a

higher current fet. A 2.5MHz trap is used to filter away any rests of the 2.5MHz sampling frequency. This is especially important if a CA3080 is used in place of the LM3080, since the CA3080 exhibited a much higher 2.5MHz sampling clock leakage during experiments. To prevent 2.5MHz leakage it is also necessary to filter and bypass the -5V supply. The 1µ bypass capacitor must be a multilayer ceramic, a tantalum capacitor is not suitable!

The format of the generated TV signal is displayed on figs.19. and 20.

The second printed circuit board has the dimensions of 100 x 190 mm^2 and is double coated (see figs 23. and 24.) The location of the components and the connections are shown on fig. 22. Most of the feed throughs from one side of the PCB to the other are made by the leads of the components, the remainder are made of short pieces of wire and are marked with small crosses on fig. 22. The connections with switches, connectors and the first PCB are numbered from 31 to 41 (the numbers in circles). The capacitor marked with an * is not necessary (second 74LS123) although holes are provided on the PCB; the stray capacitances are sufficient.

Construction and alignment

Although this scan converter is a low frequency - digital circuit, there are some things it is better to know in advance to avoid future problems. As first, digital circuits usually generate a wide spectrum of radio-frequency disturbs. As an example, the average V_{DD} current consumption of the frame memory is of the order of 150 mA, however the peaks top 1A in the form of very sharp pulses with a repetition rate of 2.5MHz! The circuits of the scan converter are not sensitive to these dis

turbs, but other units, such as the receiver, might be disturbed. It is thus necessary to mount the two printed circuits in a metal enclosure. The generated video signal is also rich of harmonics and the connection to the TV monitor should be properly shielded. On the other hand, the video signal line is also very sensitive to disturbs generated by the scan converter or by other circuits. Experience has shown that proper grounding is necessary, since disturbs are usually collected by ground loops.

It is advisable to use CMOS circuits of the new B series, especially if standard TTL circuits are to be used in place of the LS series. The memories should be fast enough: the 2102A line buffer should have an access time of 350ns or better and the 4116 frame memory chips should have an access time of 200ns or better (375ns cycle time). All the MOS circuits used are protected, so there are no valid reasons to use sockets for the integrated circuits. Personally I have had many troubles because of false contacts and "cold" solder joints in low cost sockets. Care should be taken that no short circuits are made between adiacent lines on the PCBs, which might have catastrophical consequences in some cases, for example between power supply lines. Soldering pins are used for all the connections to the printed circuit boards since multipole connectors are not easily available and are also very costly items.

The adjustment of the trimmers is not critical and no special alignment procedures are required. The circuit usually works with all the trimmers in middle position provided that a strong and clean input signal is available. The trimmers are then adjusted to optimize the various functions as already described in the text. The only exception are the two

trimmers determining the picture position and width. If the pixel period is too long, the line read cycle can not be completed during one TV line and as a consequence, the logic on PCB 2 does not work.

Conclusion

The evolution of large MOS memories has made the scan converter principle practically usable and there is no doubt that this evolution will continue in the future. 64k bit memory chips are already available suggesting a 256×256 pixel resolution scan converter to be built. PCB 1 can already drive a 64k memory module. Although the circuit presented can easily be interfaced with a microcomputer, it has the disadvantage that the frame memory can not be directly accessed by the microprocessor. On the other hand, using a microprocessor in the scan converter would probably not simplify the circuit if only the actual functions are considered. It is true that the circuit could be modified and improved in various parts, but on the other hand I think that this simple circuit can be duplicated by almost any amateur and the results that can be obtained are well worth the efforts required to build the circuit.

Nova Gorica, 30.3.1982

Nidmar Hvatja

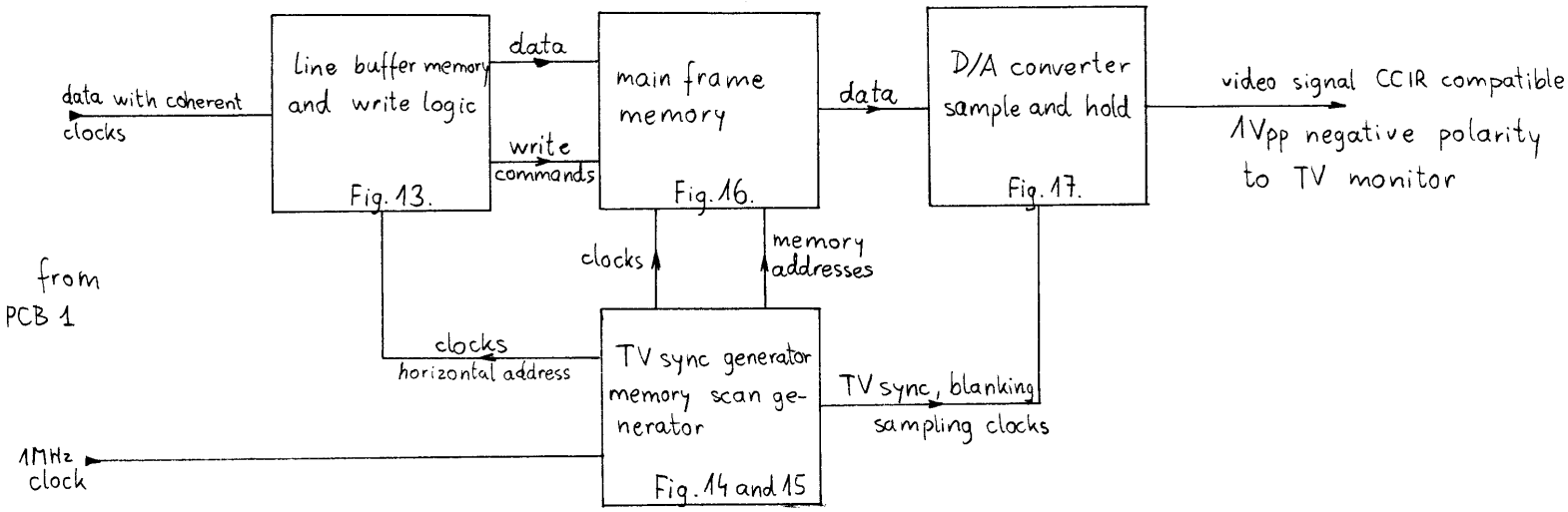

Fig. 12. - Block diagram of PCB 2.

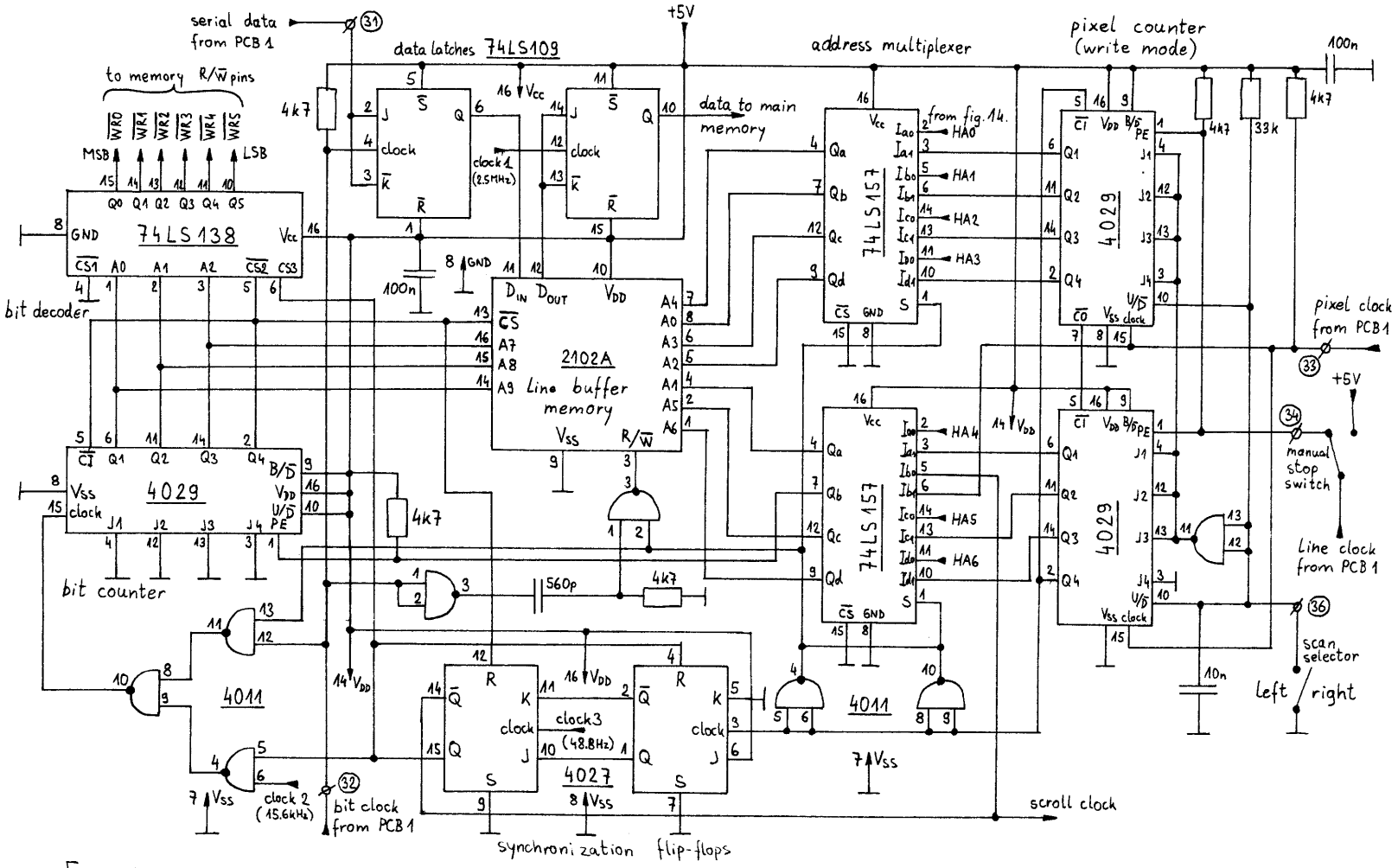

Fig. 13. – Line buffer memory and write logic

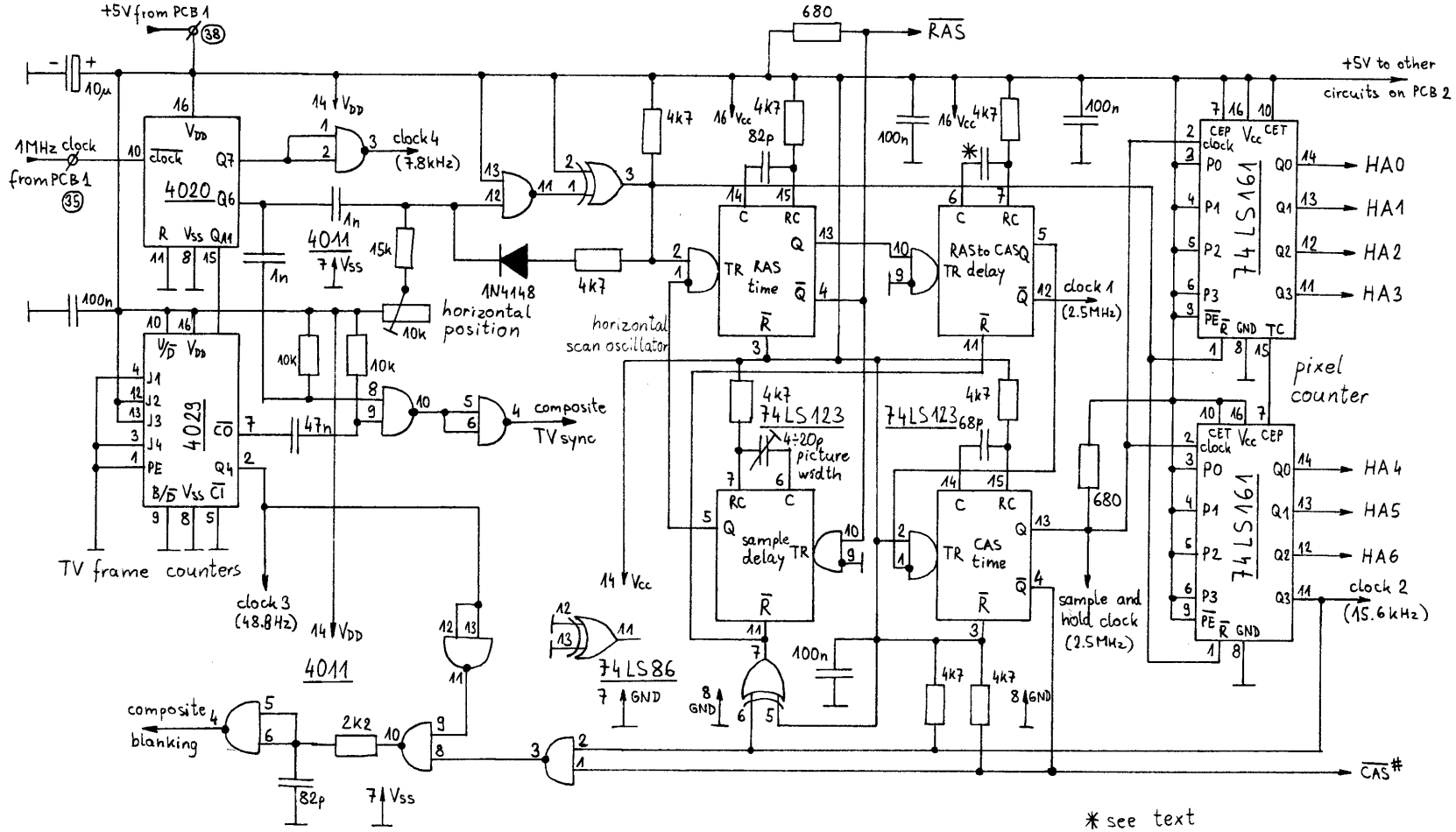

Fig. 14. – TV sync generator and horizontal memory scan generator

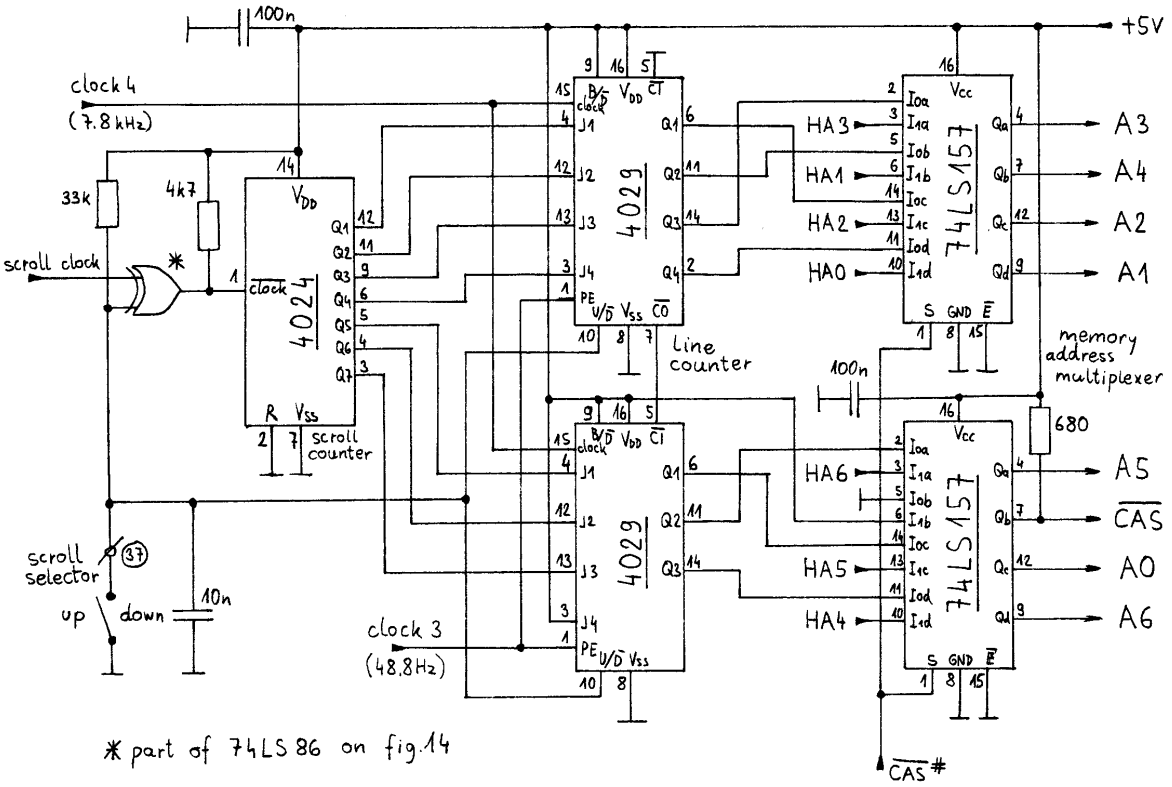

Fig. 15.- Vertical memory scan generator and address multiplexer.

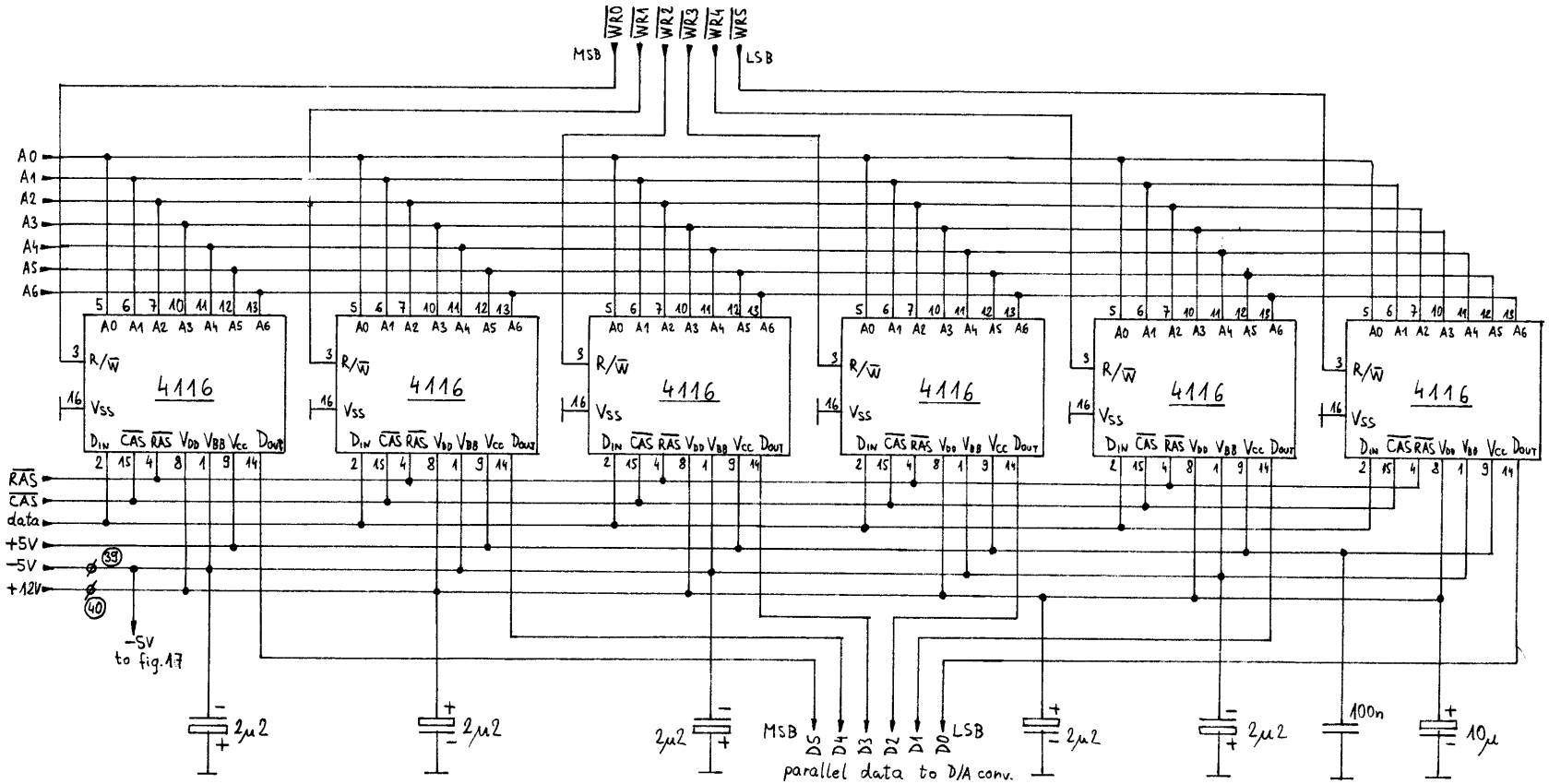

Fig. 16. - Main frame memory.

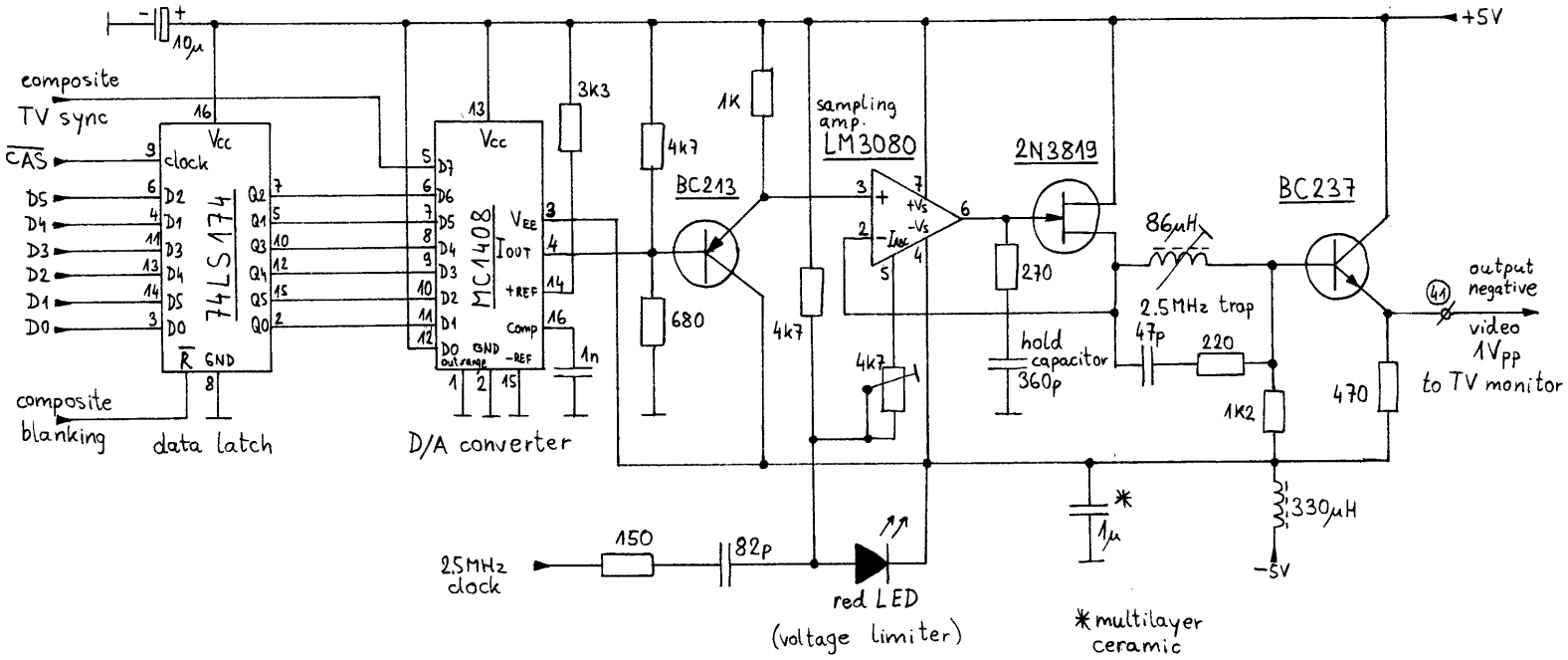

Fig. 17 - D/A converter and sample and hold.

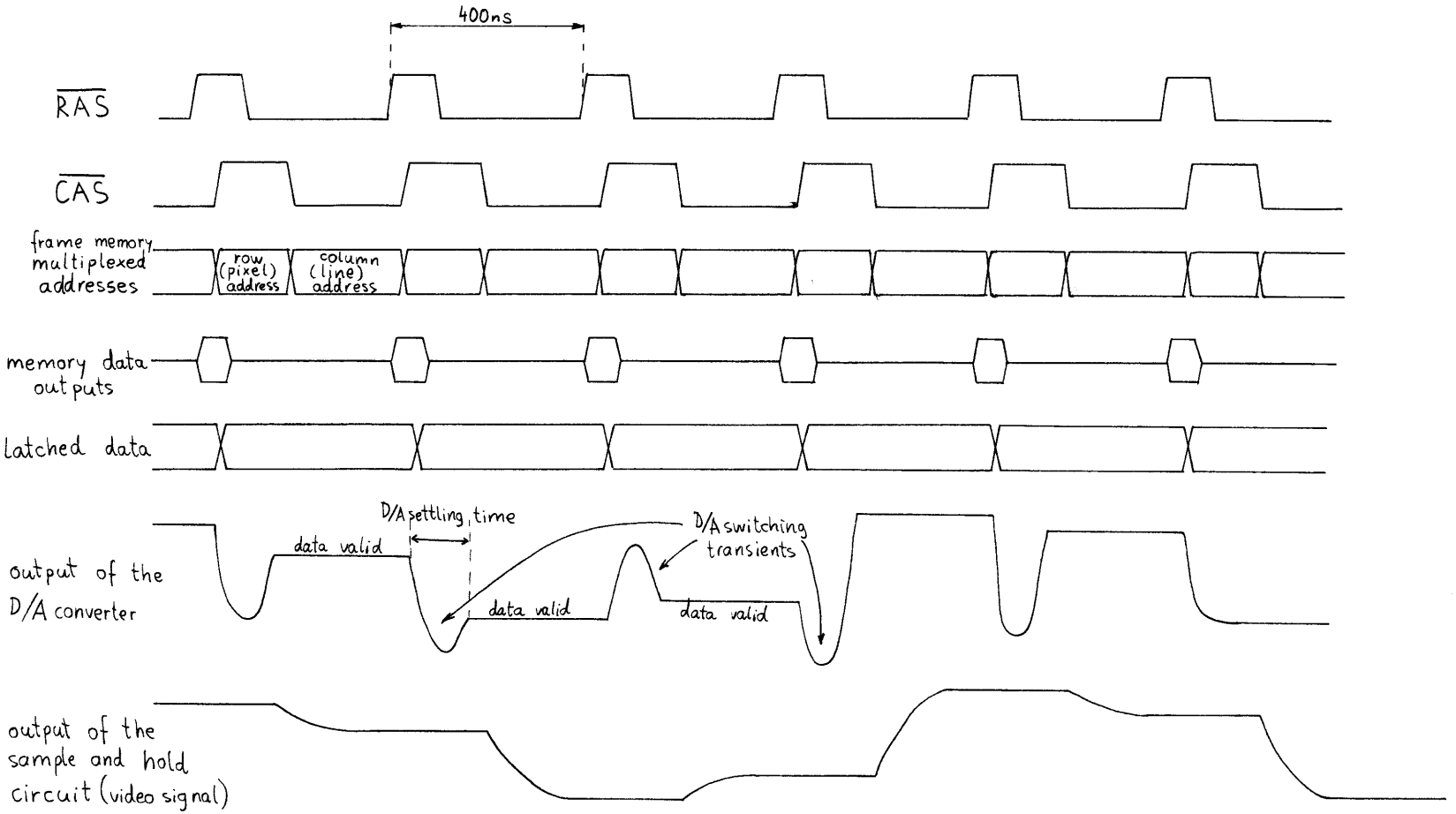

Fig. 18 - Frame memory read cycle and TV signal generation.

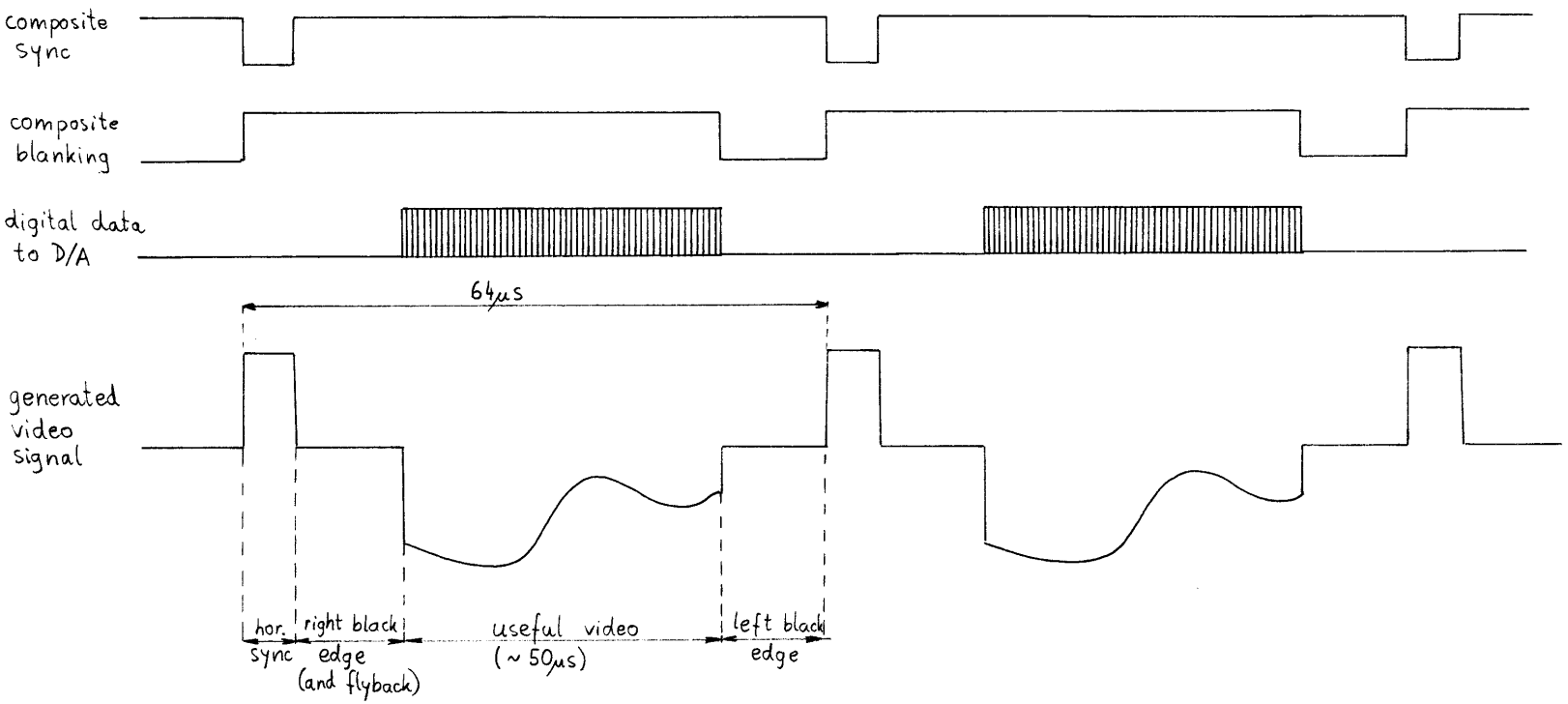

Fig. 19. - TV line format

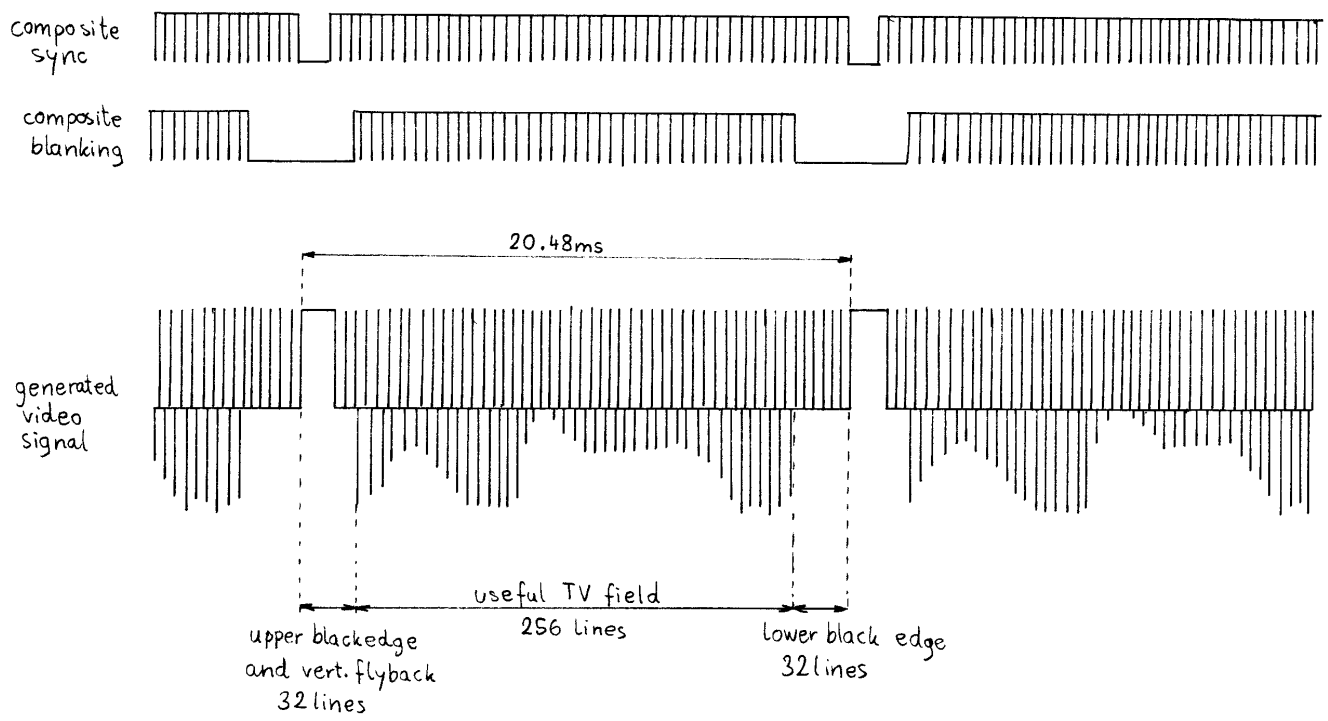

Fig. 20. - TV field format.

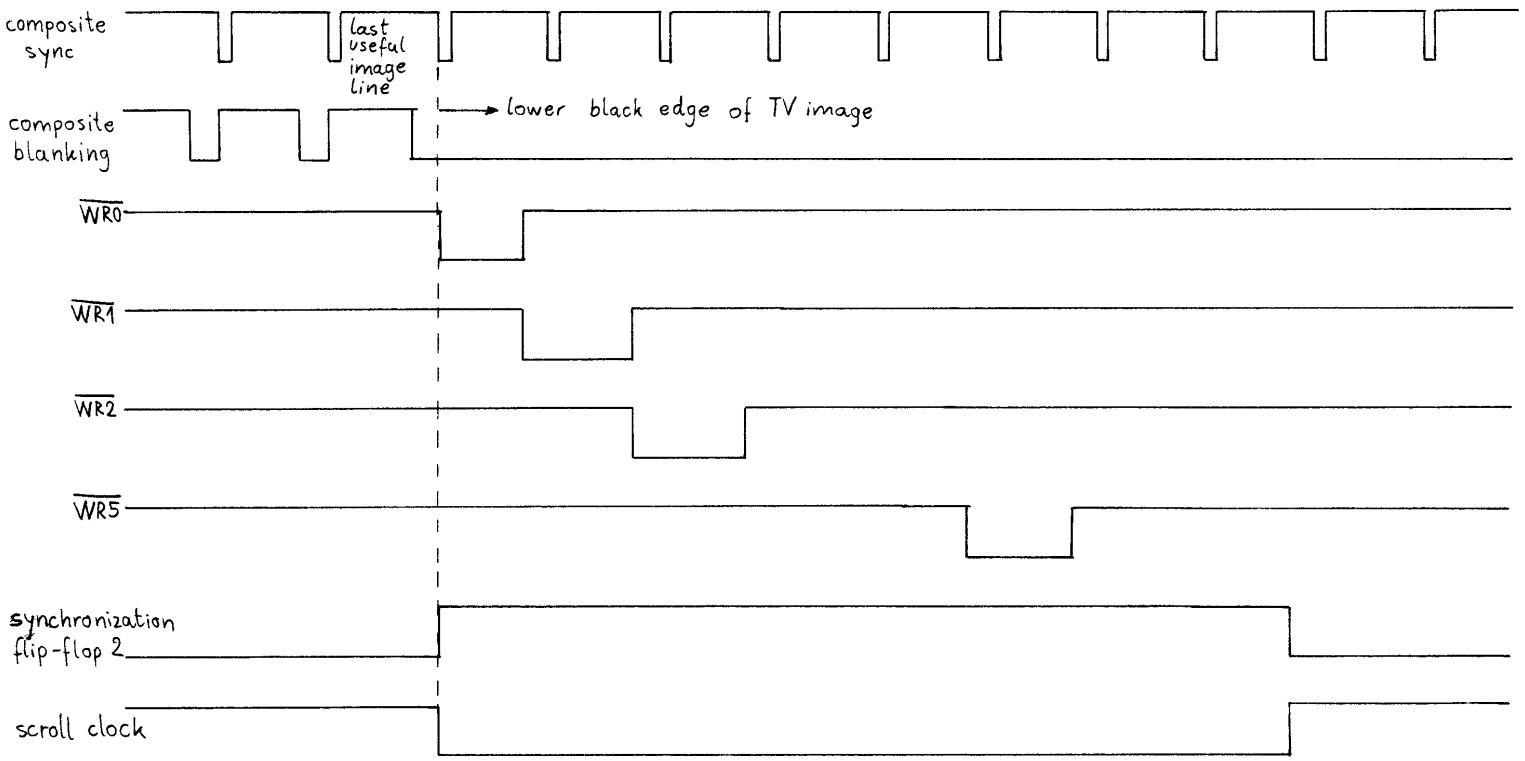

Fig. 21.- Line copy cycle.

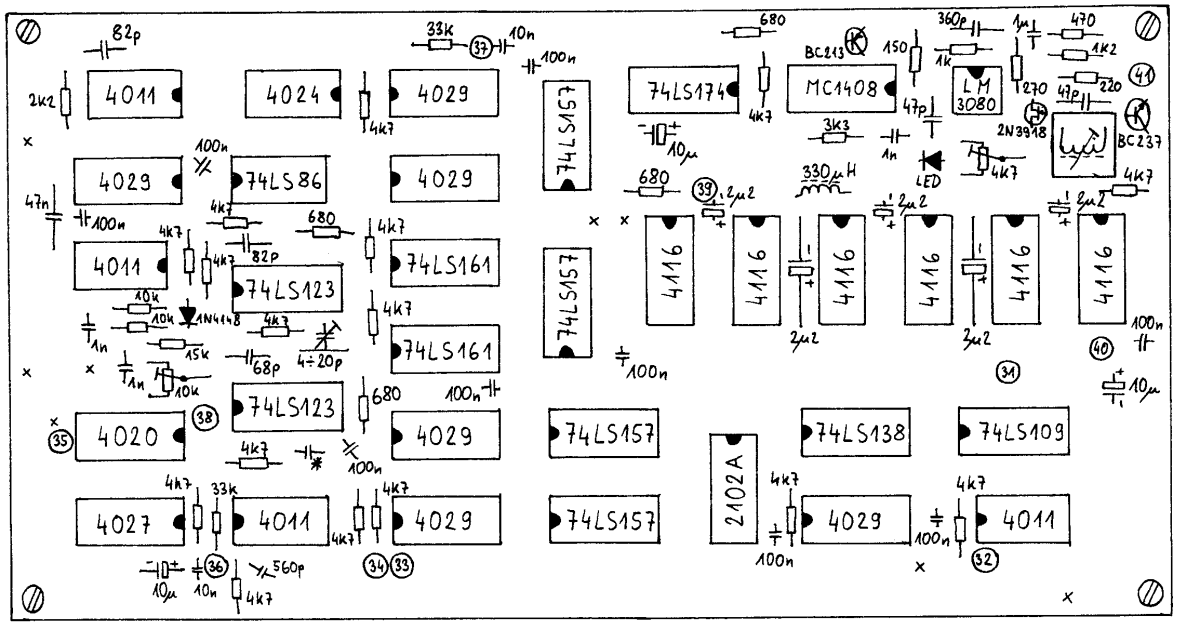

Fig. 22 - Location of the components on PCB 2.

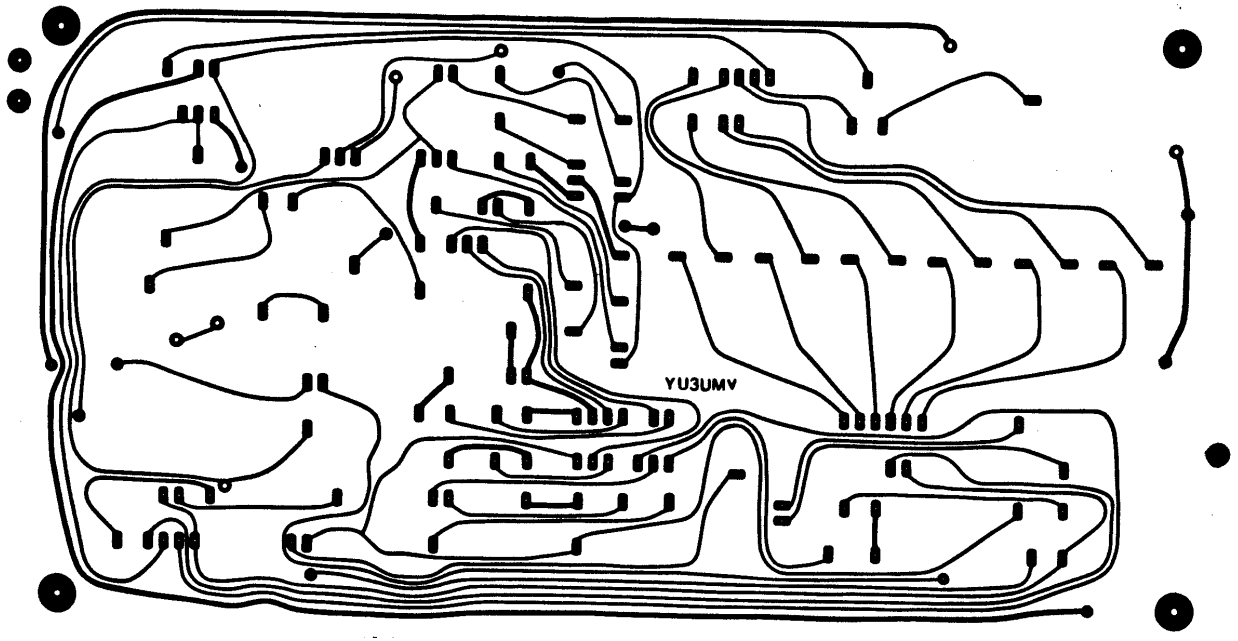

Fig. 23 - Second PCB, double coated, components side.

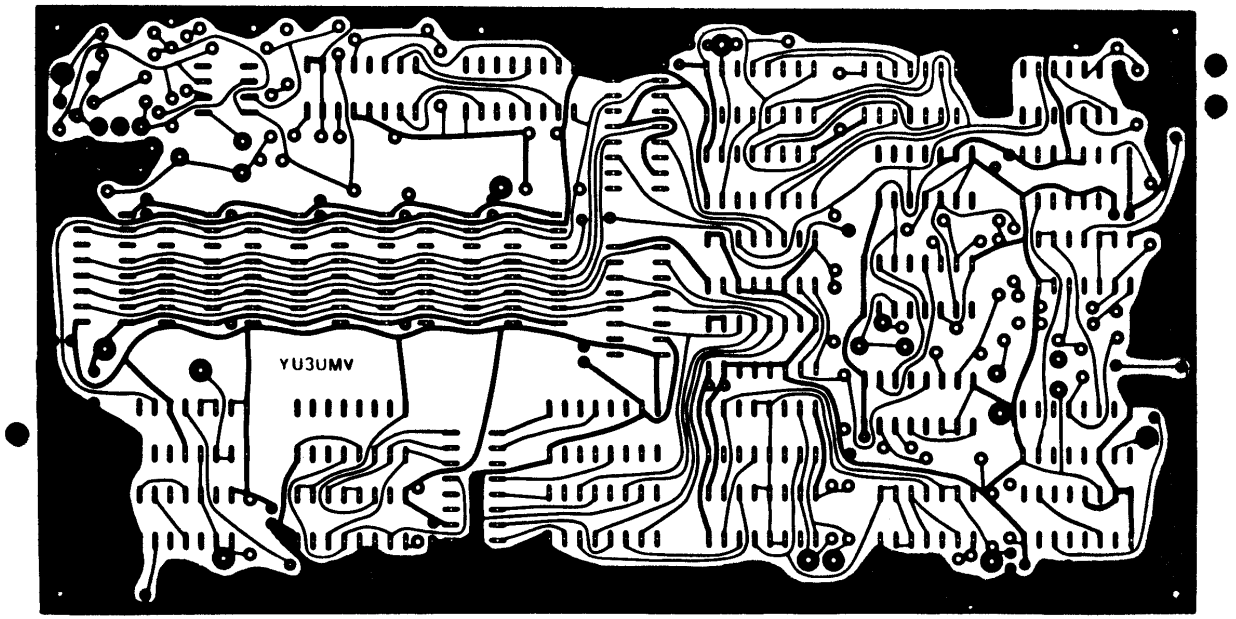

Fig. 24 - Second PCB, double coated, copper side.