2. Frame memory PCB YU3UMV 002

The frame memory unit YU3UMV 002 includes the main 64k x 6 bit frame memory, the write and read scan generators and the D/A converter to reobtain the standard analog video signal. A memory of 64k x 6 bit enables a picture resolution of 256 pixels x 256 lines with 64 grey levels. In the present circuit, one line of the frame memory is used as a buffer memory during the write operations and the remaining 255 lines compose the useful picture on the TV monitor. PCB 002 generates a 320 lines, non-interlaced TV frame. The remaining 65 lines are shared among the vertical flyback and an upper and a lower black edge on the screen. Both polarities of the video signal are provided as outputs, so the circuit is compatible with almost any CCIR TV monitor available on the market.

The serial data generated by YU3UMV 001 or another source are first converted to parallel format. To avoid disturbing the read operations from the frame memory data is written into the frame memory during the TV horizontal retrace period. The frame memory is scanned in both write and read modes by generating the addresses by a series of binary counters. I should immediately point out that it is only important to read the data out of the memory exactly in the same sequence it has been written into the memory; the physical location of the data inside the memory is not important from the user's point of view. It is thus important to immediately distinguish between external memory scanning (corresponding to the image scanning) and internal memory organization, which is also a bi-dimensional matrix. These two organizations have no

relation ship (at least in theory) and thus all the address lines are equivalent from the user's point of view except for some technical constraints for dynamic RAMs we shall discuss later.

The same circuits that generate the scanning addresses in the read mode supply also the TV blanking and synchronization pulses. These are combined with the digital video information in the D/A converter to obtain a standard analog TV video signal.

2.1. Description of the circuit

To simplify the description of the circuit the circuit diagram of the frame memory unit YU3UMV002 was divided into 4 parts, according to the block diagram on fig. 12.

2.1.1. Write logic

The write logic, displayed on fig. 13., includes the serial to parallel conversion circuit, the write cycle synchronization circuit and the write pixel counter.

The serial data originating from YU3UMV001 (or another source) are clocked in the shift register IC201. The IC202 counts the number of bits clocked into the IC201. When all the 6 data bits of a pixel have been accepted by the IC201, the IC202 generates a strobe pulse to transfer the data in the latch of the IC201. A delayed strobe pulse also resets the SR flip-flop made of two NOR gates (½ IC203) which in turn resets the IC202 counter and issues a request for a write cycle to the write cycle synchronization flip-flops (IC204).

The write command is synchronized with the raising edge of the $\overline{RAS}$ clock at the end of a TV line to perform the write cycle during the horizontal fly back. The write command also advances (or defeats) the write pixel counter, generating the write horizontal adresses WHA 0 ÷ WHA 7.

The next pixel clock pulse sets the SR flip-flop, enabling IC 202 to count the bits again and repeat the write cycle. After 256 pixels have been written into the memory, the pixel counter reaches its final state, pin 7 ($\overline{CO}$) of IC 206 goes low inhibiting further write cycles and generating a scroll clock pulse, thus introducing the new line in the image.

The following line can only be written when the write pixel counter has been reset by the line clock pulse (refer also to the timing diagram on fig. 9 published with the first part of the article).

The pixel counter can count up or down, according to the scanning of the image to be displayed. A front panel switch is provided to select either right (W → E) or left (E → W) scanning.

2.1.2. TV clocks and horizontal scan oscillator

This unit, displayed on fig. 14., includes a divider and a series of monostables to generate the various synchronization pulses, all derived from the 1MHz clock supplied by YU3UMV 001, the horizontal pixel oscillator and the read pixel counter.

The 1MHz clock is fed to IC 207 which divides it by 64 to obtain 15,625 kHz, the TV line frequency. This frequency is further divided by 32 by IC 207 and by 10

by IC 208 yielding a total division factor 320 to obtain the 48,8 Hz frame frequency. Two simple monostables, built by CMOS gates (½ IC 209), supply the composite TV synchronization pulses named $\overline{\text{TVSYNC}}$. Horizontal blanking pulses are obtained by one half of IC 210 while vertical blanking pulses are obtained by delaying the pulses present on pin 2 (Q4) of IC 208 by a flip-flop (½ IC 215). The composite TV blanking pulses are then named $\overline{\text{TVBLK}}$.

The clocks and other signals required to drive the dynamic memories are best explained by fig. 20. At the beginning of a TV line a pulse generated by ½ IC 210 (pin 4) starts the horizontal pixel oscillator built by the two monostables of IC 212. The period of the horizontal pixel oscillator can be adjusted around 200 ns. It determines the useful picture width. Considering that there are 256 pixels per line the useful line lenght is around 51,2 µs out of the 64 µs of a complete TV line, including flyback. The main design challenge was to retrive the data at a sufficiently high rate from the relatively slow available 64 k bit dynamic memories. The parameter of interest is the read cycle time and this is specified 230 ns even for the fastest 150 ns access time devices. Page mode read operation was the only possible choice.

The $\overline{\text{RAS}}$ clock is generated by the second retriggerable monostable of IC 210 (pin 12). Since the associated RC constant is quite large, the monostable is continuously in the active state while triggered by the fast pixel oscillator. In this way a long $\overline{\text{RAS}}$ read pulse is generated. The $\overline{\text{CAS}}$ clock is in turn generated by delaying (and amplifying) the pixel oscillator pulses. A SR flip-flop (½ IC 211)

generates the ASEL signal that controls the address multiplexer.

Each pulse of the pixel oscillator advances the pixel counter, generating the read horizontal addresses RHA0 ÷ RHA7. As soon as 256 pixels have been counted, a flip-flop is triggered (½ IC215) that cuts the feedback path of the oscillator. An eventual write request is synchronized with the raising edge of the $\overline{RAS}$ clock. Since the feedback of the pixel oscillator is interrupted, the write command produces a single $\overline{CAS}$ pulse. The counters, flip-flop and monostable are then reset by the next line start pulse generated by the first half of IC210 (pin4).

During the vertical flyback period the page mode cycles are shortened to a few $\overline{CAS}$ cycles to lower the memory power dissipation, since their only function is to enable write cycles.

2.1.3. Vertical scan and address multiplexer

The vertical scan generator includes the scroll counter and the line counter. These circuits are displayed together with the address multiplexer on fig. 15.

Scanning the memory in exactly the same way during write and read operations is probably the most obvious solution. Unfortunately it is quite unpractical when receiving radiometer scanned images from polar orbiting spacecrafts, since the displayed image is usually divided into two sectors, one containing old image data and the other new information being written into the memory. A much more elegant method is scrolling: new data lines are introduced at the top or at the bottom of the image field and the previous information is shifted down or up

respectively. In this way the display acts like a window moving along a radiometer scanned image. Fortunately scrolling is easy to implement in practice.

The scroll counter IC 218 supplies the vertical addresses during write operations. When a complete line is written into the frame memory, the scroll counter is incremented. The scroll counter also supplies the start address for the line counter that generates the vertical addresses during read operations. In this way data is always written in the first scanned line of the TV frame memory. This line acts like a buffer memory. Since the content of this line is continuously changing, it is made not visible by the $\overline{\text{TVBLK}}$ signal.

Whether the previous image information will be shifted up or down depends on whether the line counter is counting respectively up or down. A front panel switch is provided to select the scroll up for N→S scanned images and scroll down for S→N scanned images.

64k-bit memories require 16 address bits to select the desired location in the memory. Most 64k-bit dynamic RAMs have 8 address lines. The 16-bit address is then supplied sequentially as two consecutive 8-bit words. Since the delay between supplying the first part of the address and the second part is quite short, down to 20ns, a fast electronic switch (TTL LS), called address multiplexer, has to be used. The address multiplexer shown on fig. 15. has the additional function to switch between read and write addresses during write cycles. The address multiplexer includes eight 4-to-1 switches controlled by the two select lines : ASEL for the selection between the first and the second part of the address and R/$\overline{\text{W}}$ for

the selection between read and write addresses. The eight outputs MA0 ÷ MA7 directly drive the memory address lines.

2.1.4. Frame memory and D/A conversion

The frame memory and the D/A converter with associated logic are shown on fig. 16. The six 64k-bit dynamic memories are operated in parallel: each memory stores one bit of the six bit data word representing each pixel of the image. The data word at the output of the memory is valid only for a very short time (see also fig. 20.). A data latch, IC 231, is triggered by the raising edge of the $\overline{\text{CAS}}$ clock to extend the data through the whole cycle. The $\overline{\text{TVBLK}}$ signal resets the latch and thus forces the outputs to zero - black level.

The DAC 0800 is a current multiplying D/A converter. The output current is a fraction of the current flowing into the +REF pin 14, the fraction being determined by the digital word present at the B1 ÷ B8 inputs. B1 is the most significant bit and it is driven by the $\overline{\text{TVSYNC}}$ signal. The synchronization pulses are in this way larger than prescribed by the TV standard, however no disadvantage was noted in practice. The data word containing picture information is applied to the following 6 inputs. The last input, representing the least significant bit, is not used.

The DAC 0800 has a very fast response, the settling time of the output current is of the order of 100 ns. In this application it is much more important that it does not generate large switching transients as it was the case with older integrated D/A converters (MC1408)

and a fast (and critical) sample and hold stage at the video output can be eliminated.

The output level of IC 232 is low. A video amplifier μA733 - IC233 is used to raise the signal level to about 1,5 Vpp (loaded), suitable for most TV monitors.

2.1.5. Interface with YU3UMV001

The frame memory module YU3UMV002 requires exactly the same steering signals as the previously planned 16k × 6-bit storage module, so no modifications are necessary to the circuits on the YU3UMV 001 module. However, there are some slight differences in the connection of the resolution - zooming selector (fig. 4.) as shown on table 2. Only a three position selector is used, since the 2,4 kHz signal is no more required and the corresponding connection to Pt 107 is deleted. Since the new 64 k-bit memories do no more require a +12V supply, also Pt 126 is not connected.

It is worth noting that although the memory size has been changed, the connections to the picture format selector (fig. 5.) remain unchanged. Finally, if YU3UMV001 and 002 are to be used for APT reception only, without connections to other digital circuits, the ENABLE input Pt 116 must be grounded!

2.2. Construction of the module

The frame memory module YU3UMV002 is constructed on a double sided printed circuit board, see fig. 18. and 19.), having the same dimensions as YU3UMV001. Most of the transitions from one side to another are realized by components' leads, the remaining are marked

with a small cross on the components' location plan on fig. 17. The layout of the IC leads dictates a quite small geometry of the PCB, so extreme care is required to avoid unwanted shorts when soldering the components. In particular it is important to verify the connections below each integrated circuit on the components side of the PCB before soldering, since there will be no way to control them later!

All the MOS ICs employed are protected, so there are no valid reasons to use sockets. If you however prefer to use sockets, use only the best quality available. Low cost sockets usually cause false contacts, which are very difficult to locate in such a complex circuit!

As on YU3UMV 001 all the connections to switches, connectors and the first PCB are made through soldering pins. The only connection that requires some care is the video output. Although the video signal level is high (1.5Vpp), this is a wide band, wide dynamic range line and thus very sensitive to disturbs generated by the logic circuits. Experience has shown that such disturbs are usually collected by ground loops, so proper grounding is necessary.

2.3. Selection of the components

The main components of YU3UMV002 are listed on fig. 21. It is recomended to use CMOS ICs of the new B series. The TTL circuits are all of the LS series, since only these are fast enough and can be driven by CMOS logic at the same time.

Time determining components always cause problems because of their wide tolerances. A 2:1 spread was no-

ticed for 74LS123 dual monostables made by different manufacturers! Hence the two 74LS123 must be of the same make and possibly with the same date printed on the case.

There are a number of different 64k-bit dynamic memories available on the market. The major differences between 16 pin 64k RAMs are in the function of pin1. This pin enables a self-refresh mechanism in some memories while others have this pin unconnected. Both types may be marked 4164! The circuit YU3UMV002 was designed for memories without the self-refresh feature. 64k memories can have different internal organizations, for example the TMS 4164 (Texas Instruments) is organized as 256 rows by 256 columns while the HM4864 (Hitachi) has 128 rows by 512 columns. This is important in practice, since the HM4864 requires only half as much cycles as the TMS4164 for the refresh. Finally, each manufacturer sorts his final products in various speed groups. Memories with a row access time of 150ns or better are required in this circuit.

The maximum time between refresh is usually specified 2ms for 128 row memories and 4ms for 256 row memories. On the other hand, experiments have shown that dynamic memories are able to keep the data without refresh for many seconds at room temperature! Probably the above limit applies only for the operation at the highest allowed ambient temperature and maximum device dissipation. Further, in contrast with computer applications, 100% reliability is not required here and so a complete refresh is performed only once every TV frame (20ms, twice for 128 row memories). Also the page mode read

cycle can be made longer than the maximum allowed, usually 10μs. The power dissipation and thus the operating temperature of the memories are very low in this circuit, since they depend mainly on the number of $\overline{RAS}$ cycles per second, which is very low due to the page mode addressing.

Modern dynamic memories are usually specified fully TTL compatible. Unfortunately this does not necessarily mean that TTL LS circuits can directly drive highly capacitive memory clock and address lines. In particular, the active pull-up of the LS ICs may not be sufficient and an external pull-up resistor (680Ω ÷ 1,5kΩ) may be required. I have never had such problems with the TMS4164, however I had had many problems with previous circuits. Both LS TLL circuits and dynamic memories exhibit large variations of these parameters from manufacturer to manufacturer.

All the electrolytic capacitors are tantalum drops. The 100nF bypass capacitors are ceramic discs or multilayer ceramic. All the other capacitors are plastic foil types, since cheap ceramic capacitors usually have a too high temperature coefficient.

2.4. Alignment

Since the YU3UMV 002 module receives the supply, clocks and steering signals from the YU3UMV001 module, it is obvious that the 001 module should already have been tested, at least the power supply and the 1MHz oscillator. There are only two trimmers on the second PCB. It is recomended to start the alignment with R201 (horizontal position) at the minimum resistive value and

with C201 (horizontal width) in middle position. After switching on the modules, a pattern of the random initial memory content should appear on the TV monitor, probably shifted to the left on the TV screen. Now the two trimmers can be aligned for the correct position and width of the image.

Note that the adjustment of the image width has precise limits. If C201 is completely misaligned, you may not obtain any image at all! After adjusting R201 and C201, L101 on the first PCB may then need to be realigned, to eliminate eventual interferences and/or difficulties in the synchronization of the TV monitor.

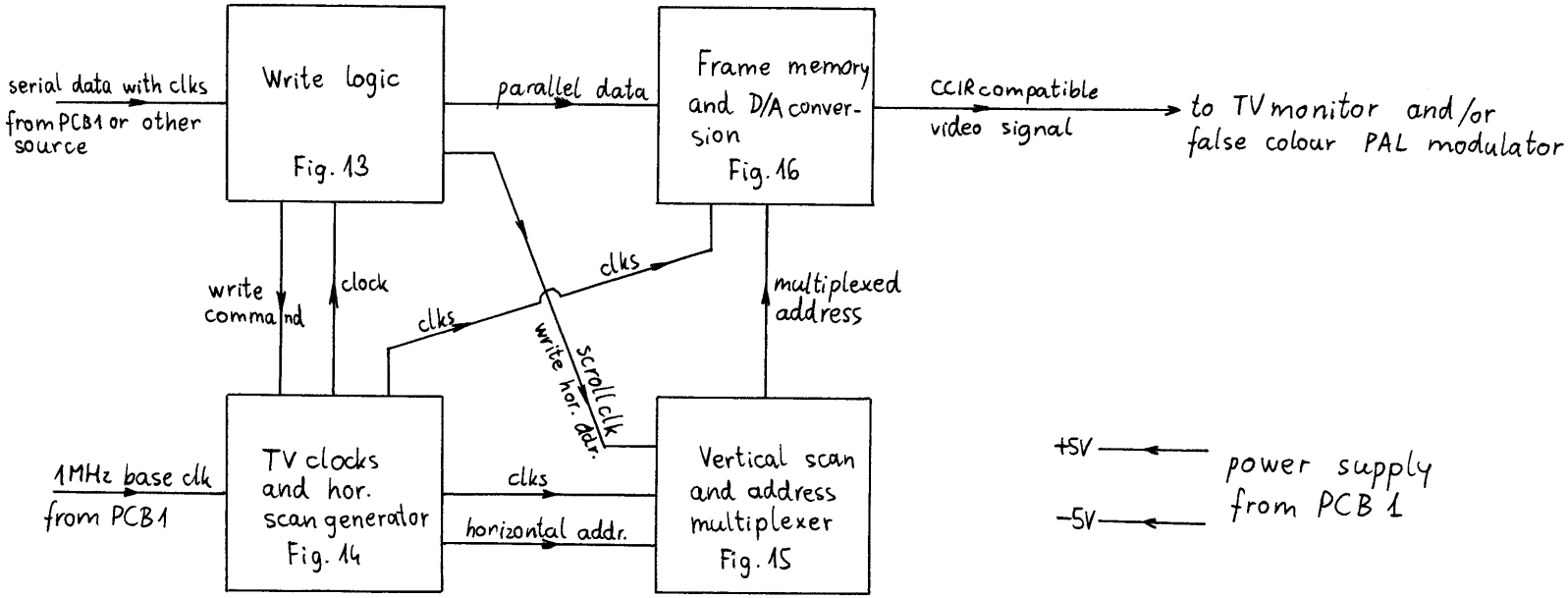

Fig. 12 - Block diagram of the second PCB.

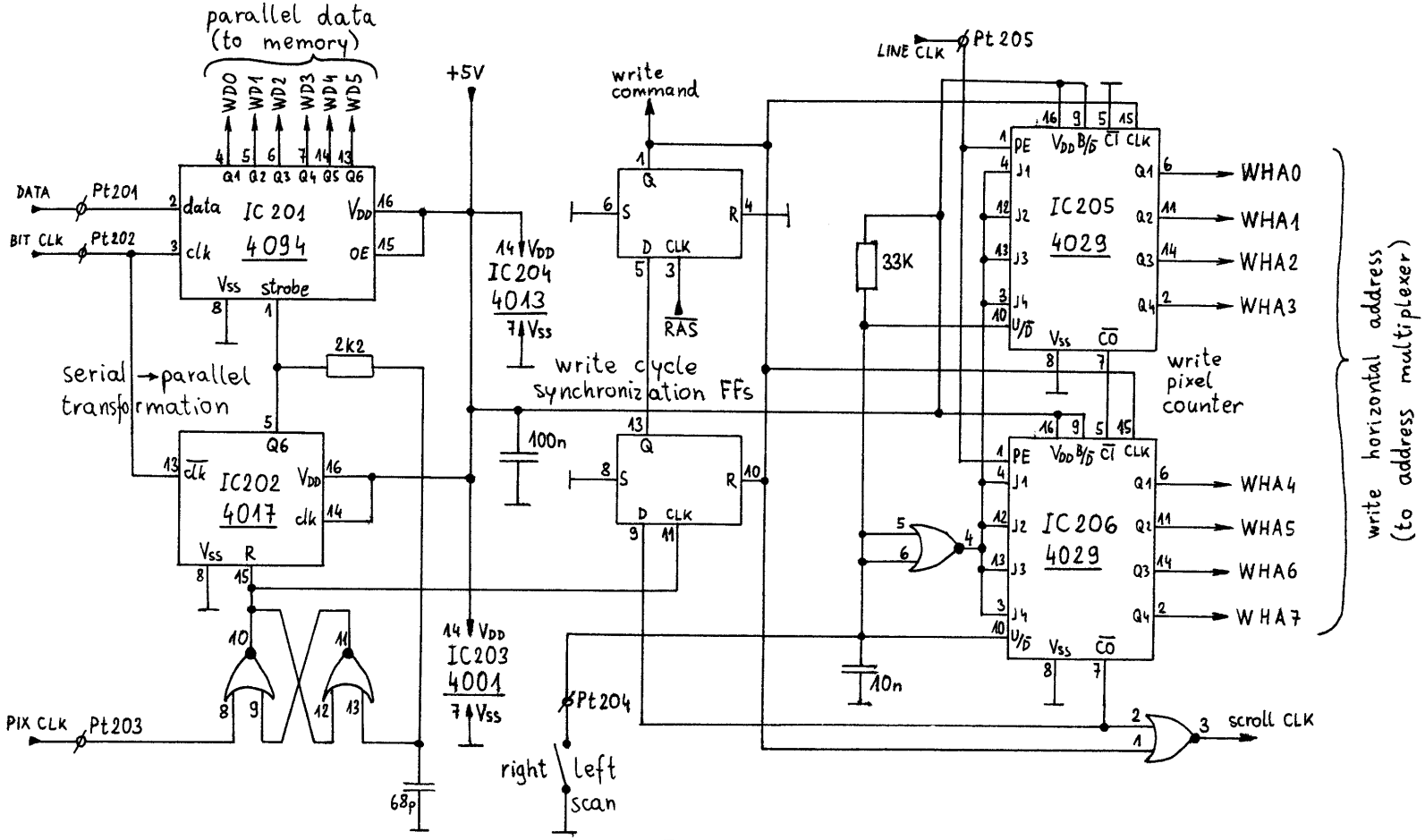

Fig. 13 - Write logic

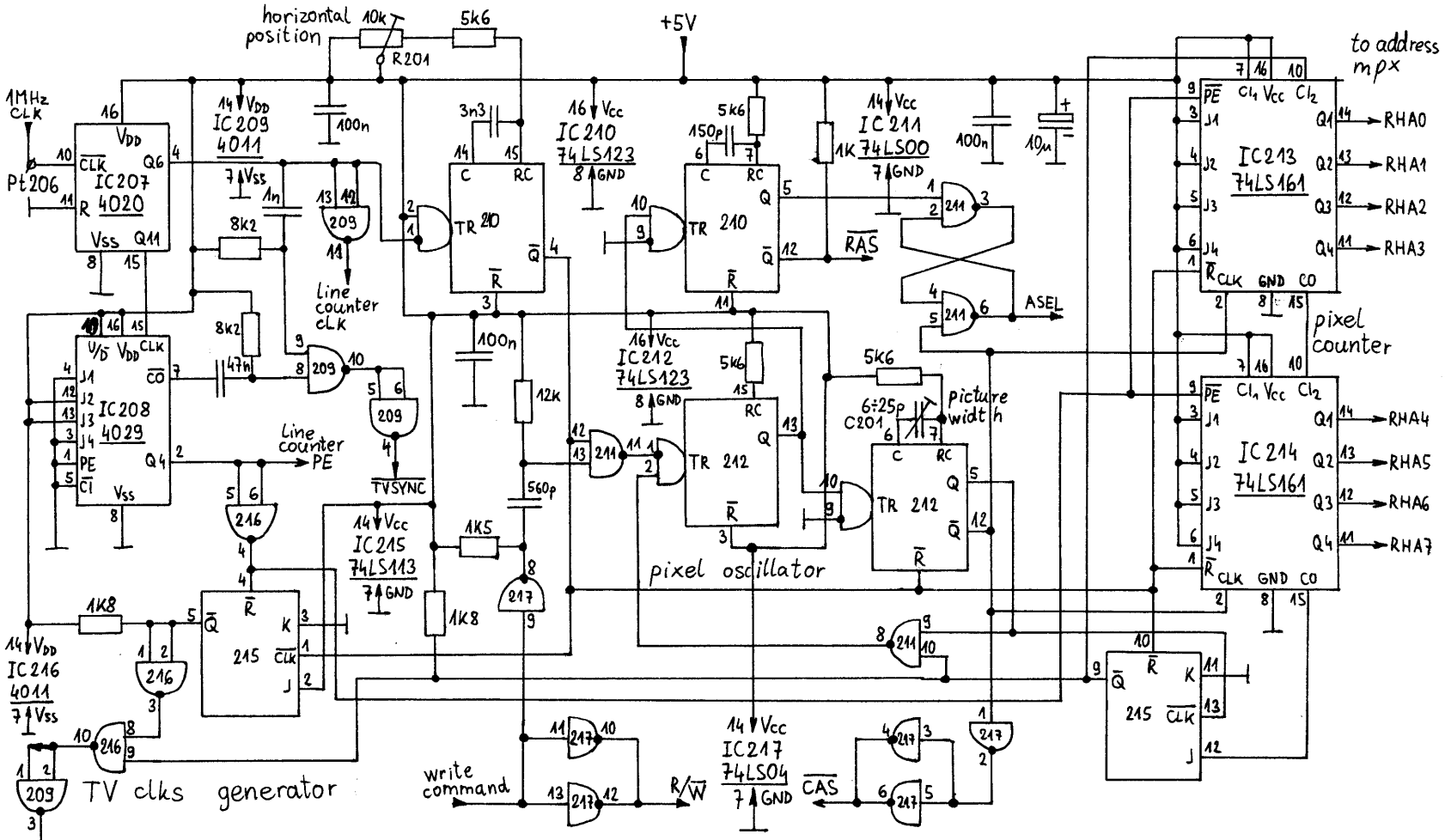

Fig. 14 - TV clocks and horizontal scan generator.

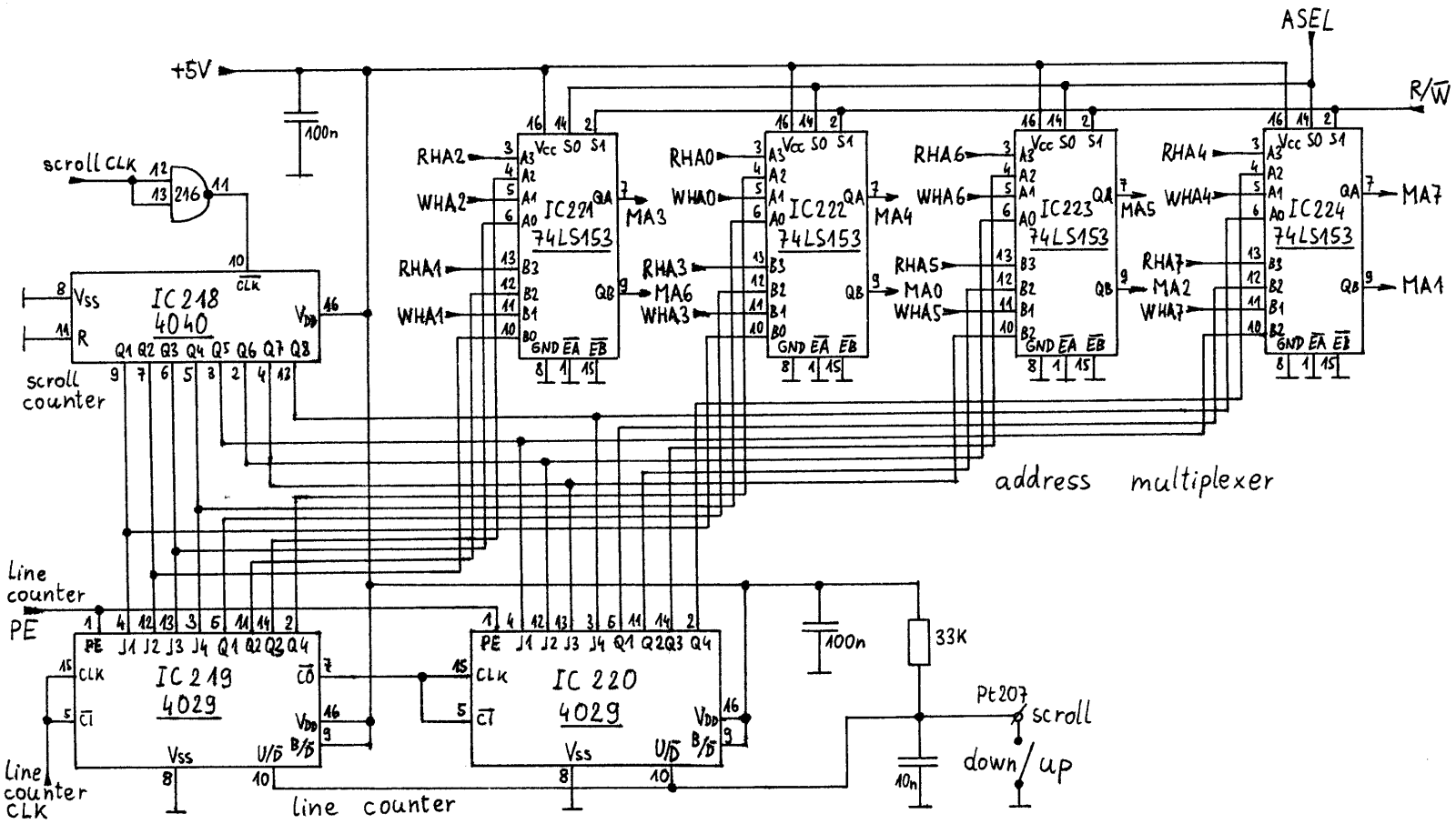

Fig. 15 - Vertical scan and address multiplexer.

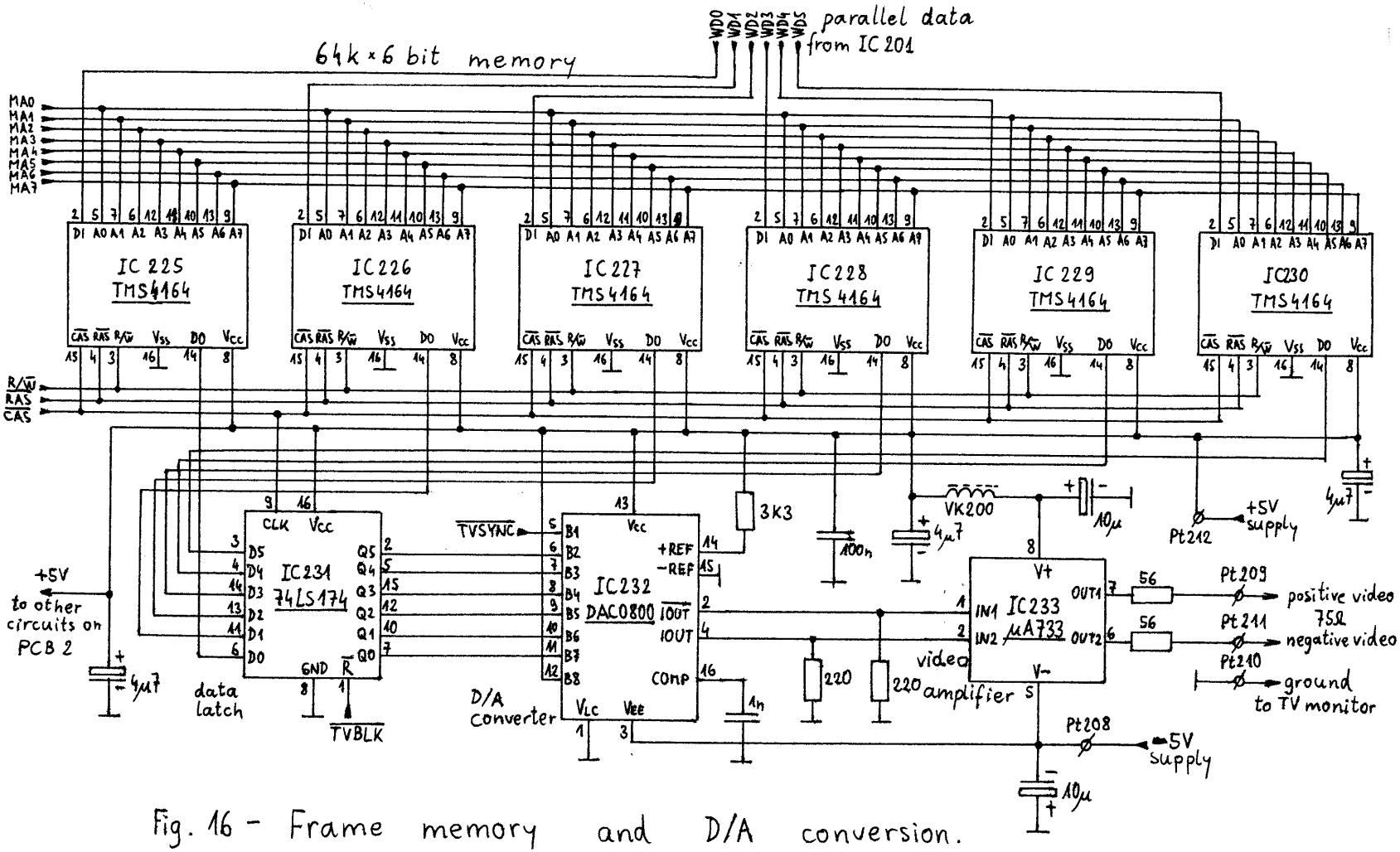

Fig. 16 - Frame memory and D/A conversion.

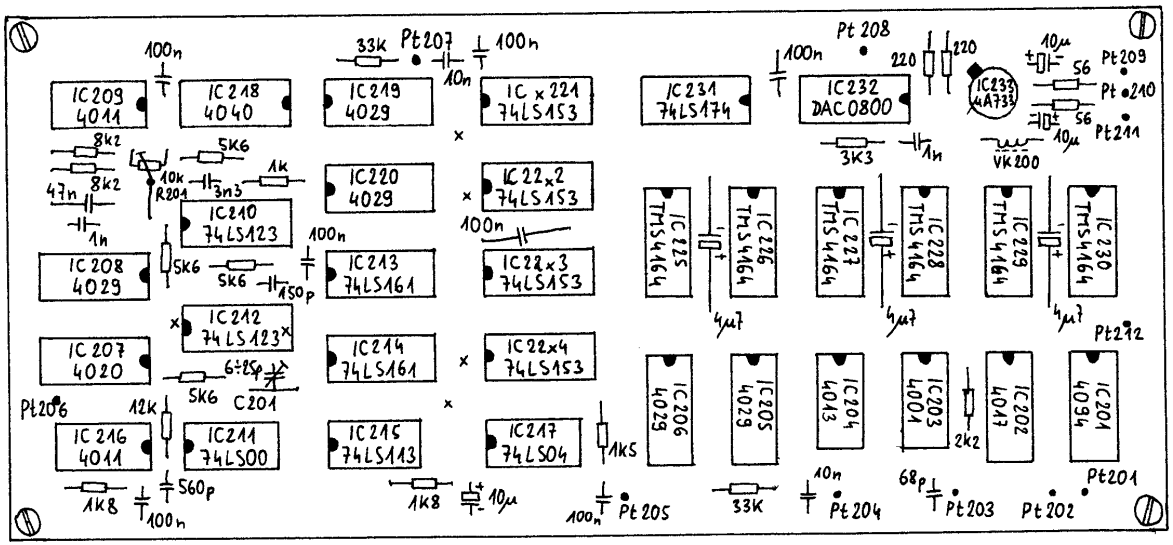

Fig. 17. - Location of the components on PCB 2.

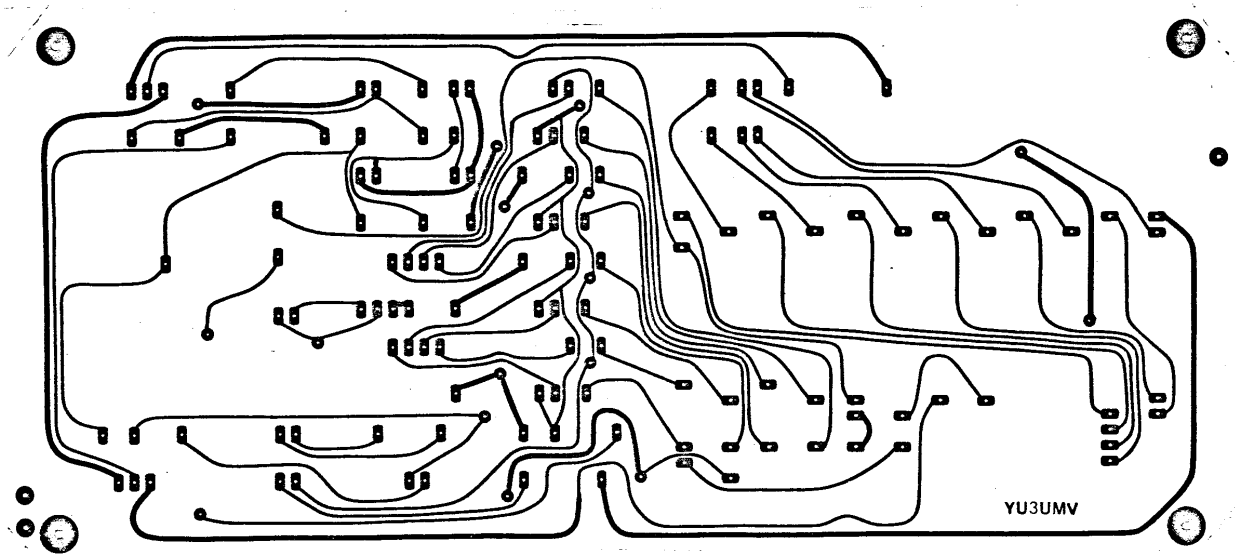

Fig. 18 - Second PCB, double coated, components side.

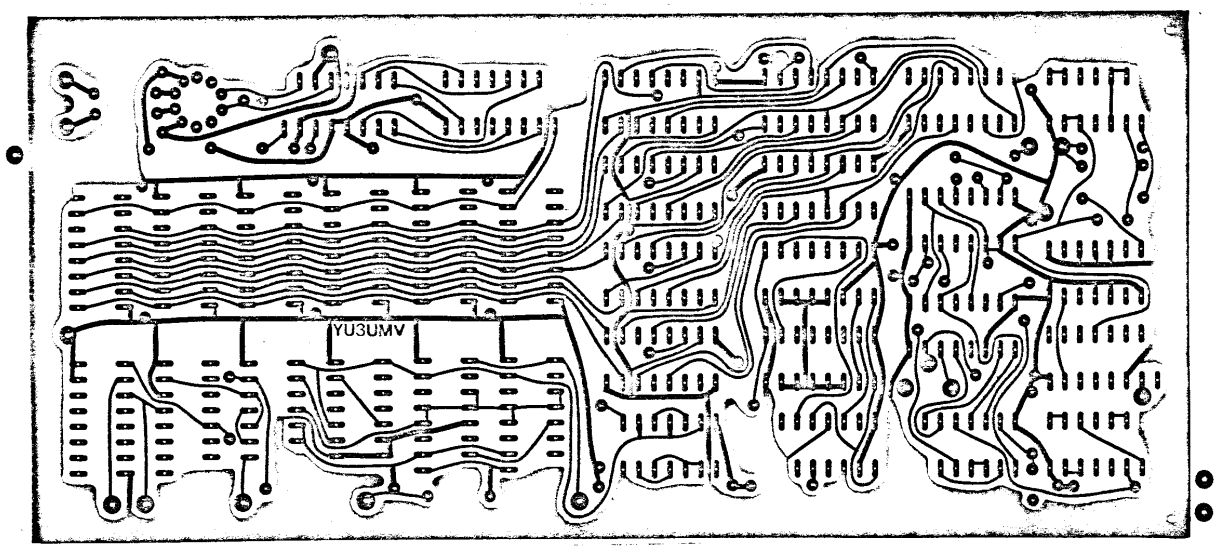

Fig. 19 – Second PCB, double coated, copper side.

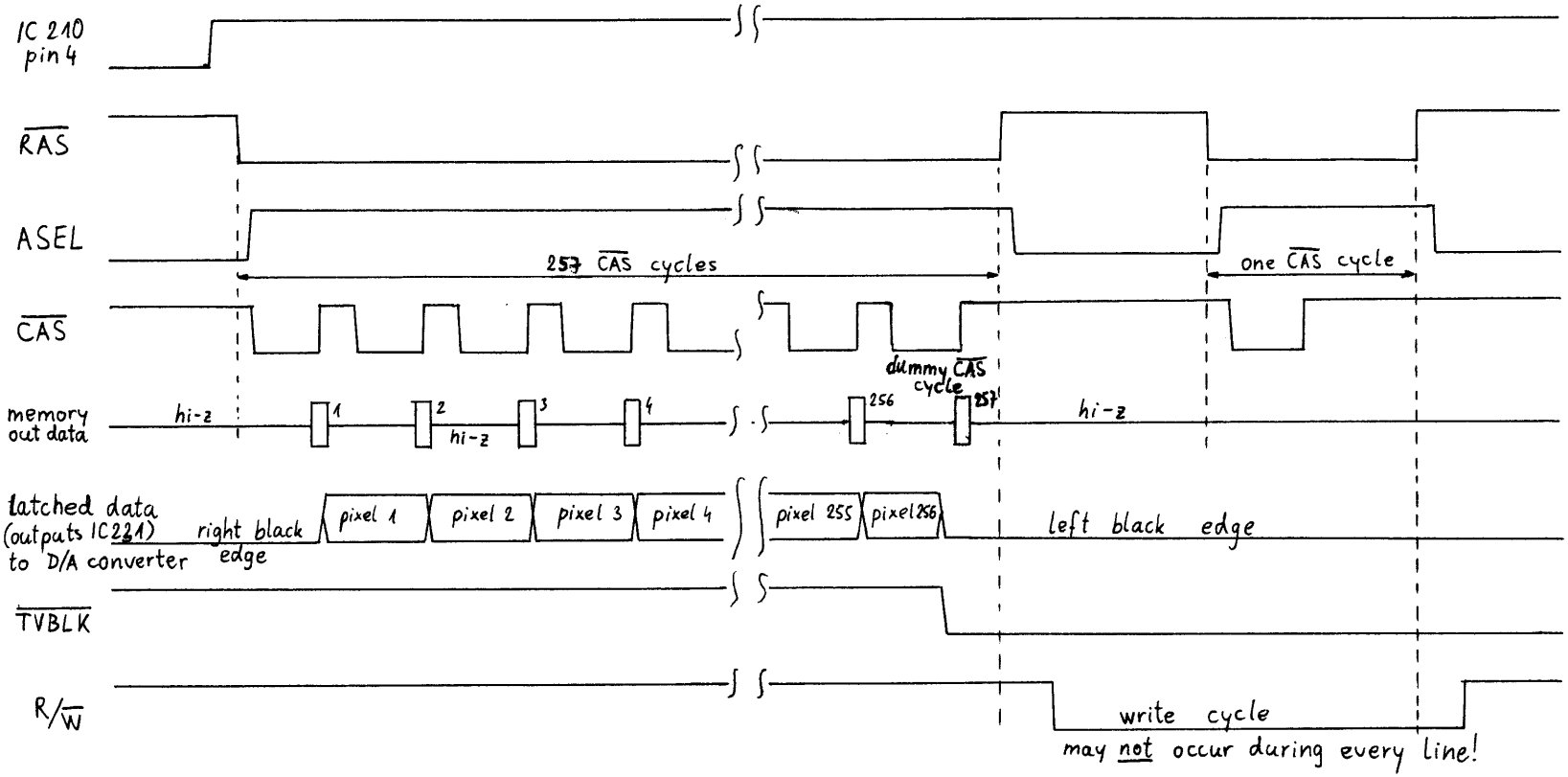

Fig. 20 - Read and write operations with the frame memory.

Fig. 21. - List of special components

IC 201	4094	CMOS 8 bit shift register with latch
IC 202	4017	
IC 203	4001	
IC 204	4013	
IC 205, 206, 208, 219, 220	4029	
IC 207	4020	
IC 209, 216	4011	
IC 210, 212	74LS123	see text!
IC 211	74LS00	
IC 213, 214	74LS161	
IC 215	74LS113	
IC 217	74LS04	
IC 218	4040	
IC 221, 222, 223, 224	74LS153	
IC 225, 226, 227, 228, 229, 230	64k dynamic memories TMS 4164-15 or HM 4864-2, 150ns access time, other memories could also be used, for further information consult the text!	
IC 231	74LS174	
IC 232	DAC 0800	D/A converter
IC 233	μA733	video amplifier, TO-99 metal can!

R 201	10k lin	trimmer 5/10mm pin spacing
C 201	6÷25p	trimmer, plastic foil or ceramic

zooming - resolution switch bit clk	sampling frequency	Meteosat WEFAX	Noaa * APT	Meteor 240 lines/min	Meteor # 120 lines/min
19.2 kHz	2400 Hz	x 2	x 2	x 2	
9.6 kHz	1200 Hz	x 1	x 1	x 1	x 2
4.8 kHz	600 Hz		VIS + IR		x 1
2.4 kHz	300 Hz				

* Meteo/Noaa switch in Noaa position

External 2400 Hz synchronization required

Table 2 - Image formats displayed with 64 k byte memory.