13cm PSK transceiver for 1.2Mbit/s packet radio

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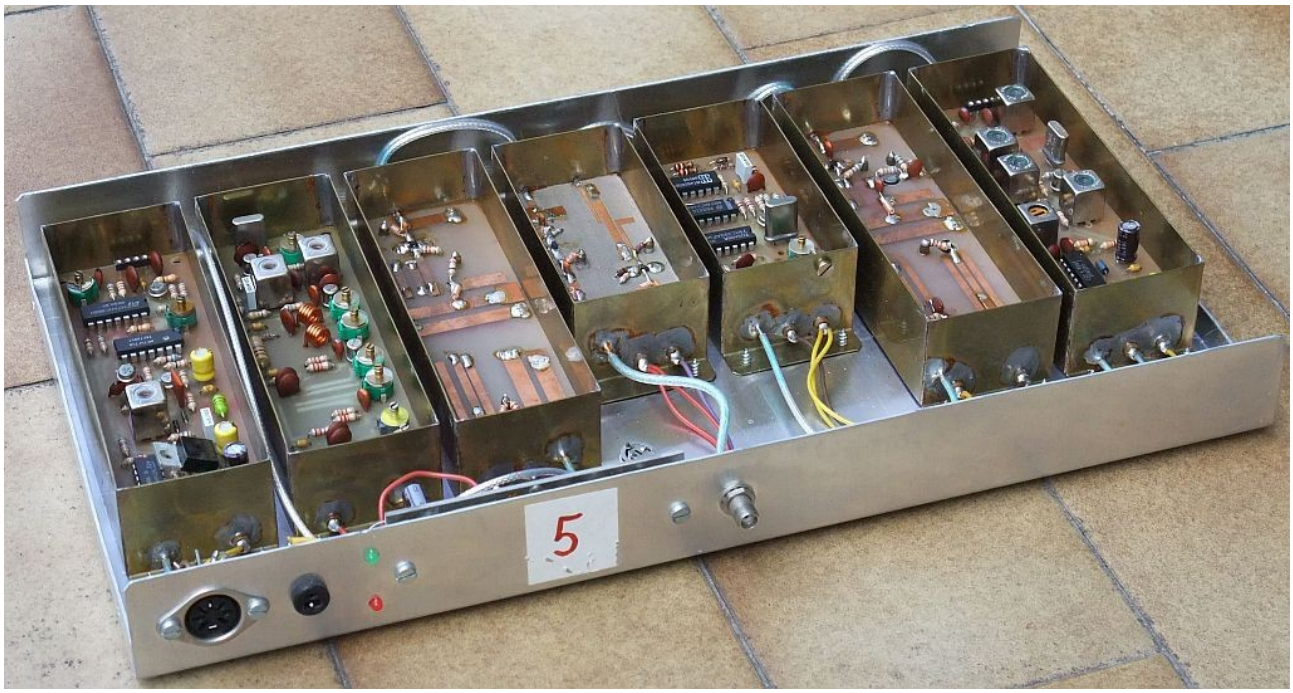
1. Introduction

The choice of a transceiver design for high-speed packet radio is not simple. Is it better to use an apparently simpler FM transceiver or to go for a more sophisticated PSK transceiver? Both choices have their advantages and disadvantages and at this time it is difficult to predict which one will become more practical. However, increasing the transmission speed both the signal bandwidth and the radio range need to be considered.

Increasing the data speed beyond about 100kbit/s, the resulting signal bandwidth is only acceptable at microwave frequencies. The transmitter power available at microwave frequencies is small and expensive. Therefore the radio range becomes a limitation even for line-of-sight terrestrial packet-radio links. A PSK transceiver with a coherent detector offers a radio range that is between 5dB and 15dB larger and a signal bandwidth that is less than half when compared with a FM transceiver.

In packet radio the main problem of a PSK transceiver is the initial RX signal acquisition. The latter is a function of the carrier frequency uncertainty. In a simple bi-phase PSK (BPSK) system with 0/180 degrees modulation, the initial signal acquisition requires a complicated searching loop, if the frequency error exceeds 10% of the bit rate. Quadri-phase PSK (QPSK) allows a further halving of the signal bandwidth at the expense of a much more sophisticated demodulator design and an even more critical initial signal acquisition.

Therefore PSK becomes simple at high data rates. On the other hand, the signal acquisition of low-Earth orbit amateur packet-radio satellites transmitting at only 1200bit/s PSK is very difficult. This unfortunate PSK design made radio amateurs believe that PSK is not suitable for packet radio, being just an unnecessary complication at low data rates like 1200bit/s.



In this article a successful 13cm BPSK transceiver design will be described. In the 13cm amateur band, the sum of the frequency uncertainties of both receiver and transmitter is at least 10kHz using top quality temperature-compensated crystal oscillators. A real-world figure is 100kHz frequency uncertainty that requires a MINIMUM bit rate of about 1Mbit/s!

With the above restriction, a convenient choice is to use 1.2288Mbit/s for packet radio. This figure can easily be obtained with standard baud-rate crystals, being the 32nd multiple of 38.4kbit/s or the 1024th multiple of 1200bit/s. Of course the described transceiver can also be used for other digital data transmissions that require megabit rates, like compressed digital television transmission.

2. 13cm PSK transceiver design

Since the above mentioned PSK modulation is relatively unknown to most radio amateurs, the 13cm PSK transceiver block diagram will be discussed first. The same form of PSK modulation, namely 0/180 degrees BPSK, allows many different transceiver concepts. For example, a PSK signal may be generated at an IF frequency and then up-converted to the final transmitter frequency. A PSK signal can also be generated directly at the final frequency and even after the transmitter power amplifier. Finally, a PSK signal can also be fed through frequency multiplier stages, but here one should not forget that the PSK modulation phase angles are multiplied by exactly the same factors as the carrier frequency.

A PSK demodulator may be coherent or non-coherent. A coherent PSK demodulator offers a larger radio range, but requires a local carrier regeneration. A PSK signal is demodulated coherently by multiplication with the regenerated carrier in a balanced mixer. Carrier regeneration requires a nonlinear processing of the PSK signal (in the case of BPSK this may be a frequency doubler) and a narrow bandpass filter (usually in the form of a phase-locked loop).

A PSK signal may be demodulated at a convenient IF frequency or directly at the receiver input frequency. A PSK receiver can be designed as a direct-conversion receiver just like a SSB receiver. Carrier regeneration may be performed by a squaring loop (frequency doubler) or by a Costas loop. Just like SSB, all PSK demodulators are very sensitive to small carrier frequency inaccuracies.

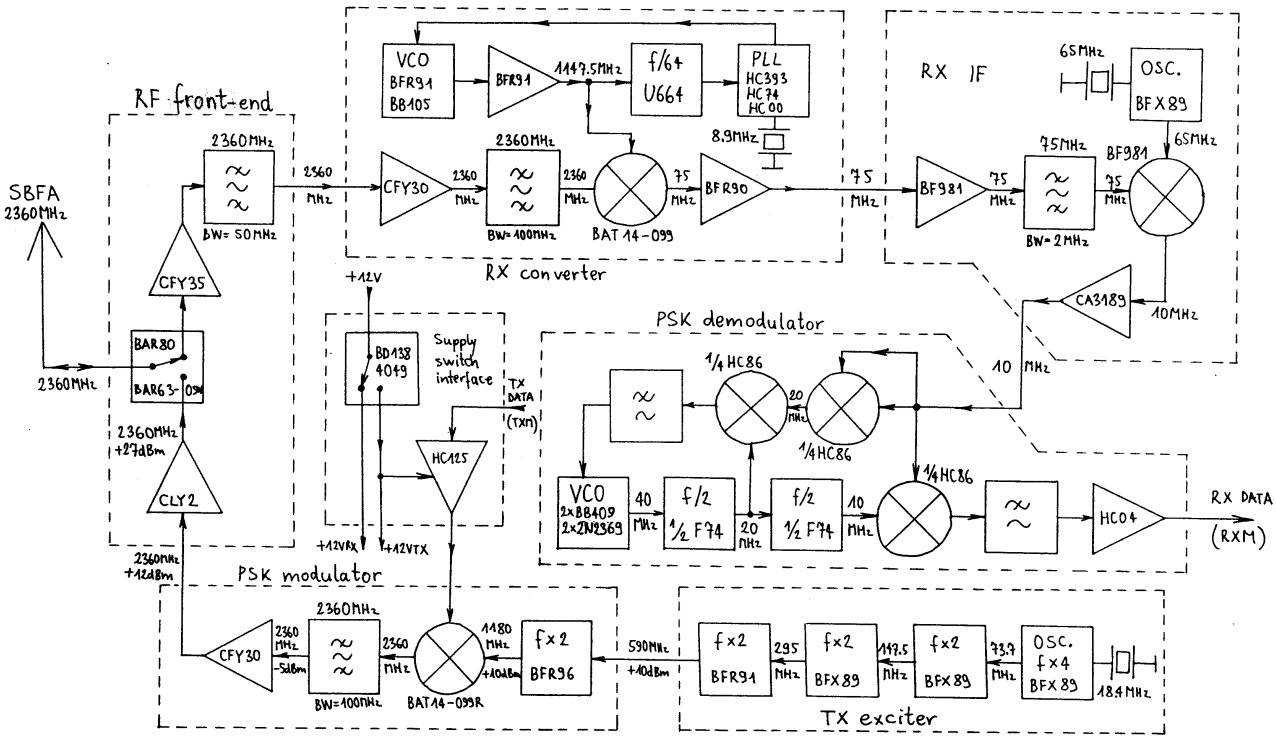


Fig. 1 – 13 cm PSK transceiver block diagram (2360MHz / 1.2288 Mbit/s).

The block diagram of the described 13cm PSK transceiver is shown on Fig.1. The transmitter includes a crystal oscillator followed by a multiplier chain. The PSK modulator - balanced mixer operates at the final transmitter frequency and generates the desired signal directly. Modern semiconductor devices provide high gains per stage. The mixer is followed by just two amplifier stages at 2.36GHz to obtain about 0.5W of microwave power.

The receiver includes a double down-conversion with the corresponding

intermediate frequencies of 75MHz and 10MHz. The 10MHz coherent PSK demodulator is a squaring loop PLL. Although the receiver and the transmitter circuits are almost completely independent, the 13cm PSK transceiver is intended for standard CSMA (carrier-sense multiple access) simplex operation as usual for packet radio. Therefore the transceiver includes a PIN antenna switch and all of the remaining RX/TX switching is completely electronic as well. The RX/TX switching delay is in the range of 2ms and is mainly caused by the turn-on delay of the transmitter crystal oscillator.

3. TX exciter 590MHz / +10dBm

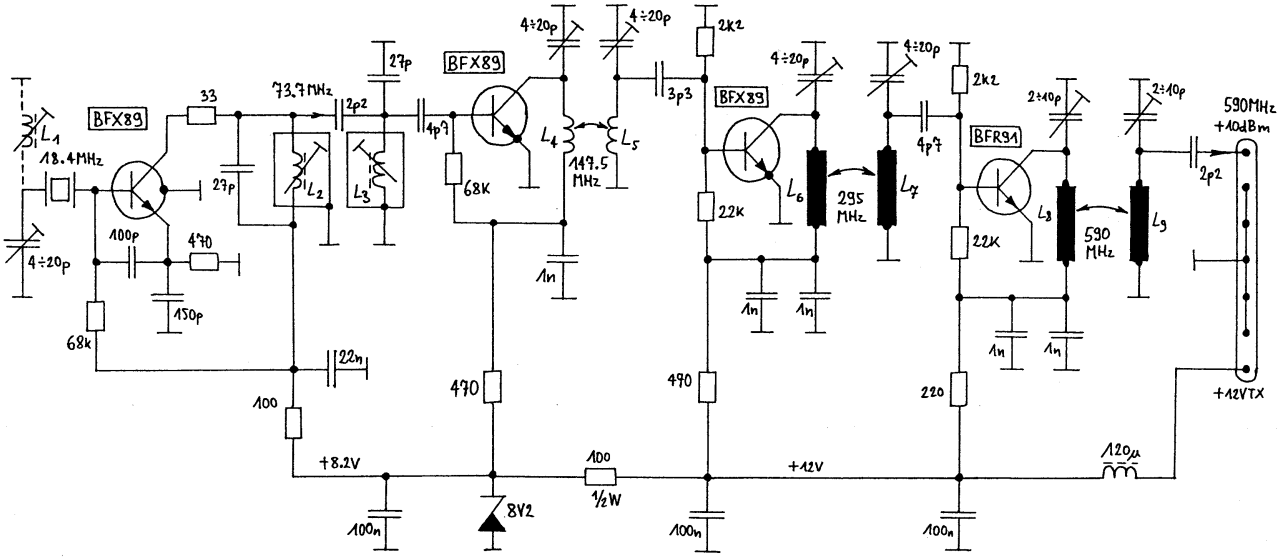


Fig. 2 - TX exciter circuit diagram.

The circuit diagram of the transmitter exciter is shown on Fig.2. The exciter includes a crystal oscillator operating around 18.4MHz, followed by a multiplier chain. The exciter includes multiplier stages up to 590MHz. These are followed by additional multipliers located in the following module, the PSK modulator, mainly because of the different construction technology. A PLL synthesizer is not recommended in the exciter, since it was found difficult to isolate the PSK modulator from pulling the VCO frequency.

The oscillator uses a fundamental resonance crystal, since fundamental resonances have a lower Q than overtone resonances. The turn-on delay of the transmitter crystal oscillator can be reduced in this way. The transmitter crystal oscillator is turned off when receiving, since its fourth harmonic could disturb the first IF at 75MHz. For operation at 2360MHz, a "computer" crystal for 18.432MHz can be tuned to the desired frequency with a series capacitive trimmer. Using different crystals for other frequencies, a series inductivity L1 may be required in place of the capacitive trimmer.

The oscillator transistor is also used as the first multiplier, since the output circuit (L2 and L3) is tuned to the fourth harmonic of the oscillator frequency. Three additional frequency-doubler stages are required to obtain about 10mW at 590MHz. The first doubler stage uses air-wound, self-supporting coils L4 and L5, while the remaining two doubler stages use "printed" inductors L6, L7, L8 and L9. The supply voltage for the oscillator and the first doubler stage is stabilized by a 8V2 zener diode.

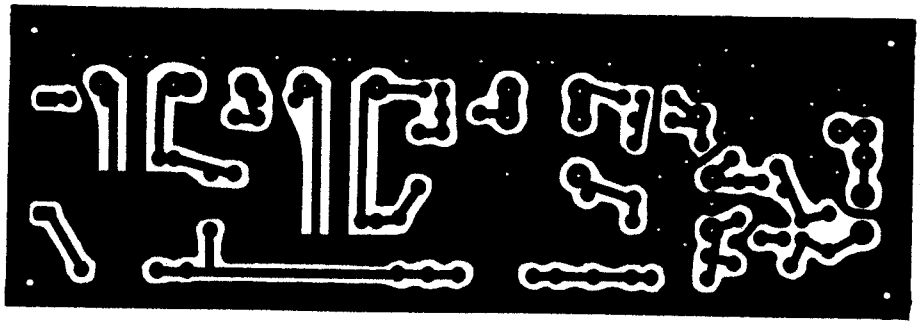


Fig. 3 - TX exciter PCB (single-sided 0.8mm glassfiber-epoxy).

The transmitter exciter is built on a single-sided PCB with the dimensions of 40mmX120mm, as shown on Fig.3. The PCB is made of 0.8mm thick glass-fiber-epoxy laminate to shorten the wire leads of the components and in this way reduce the parasitic inductances. The component location of the transmitter exciter is shown on Fig.4.

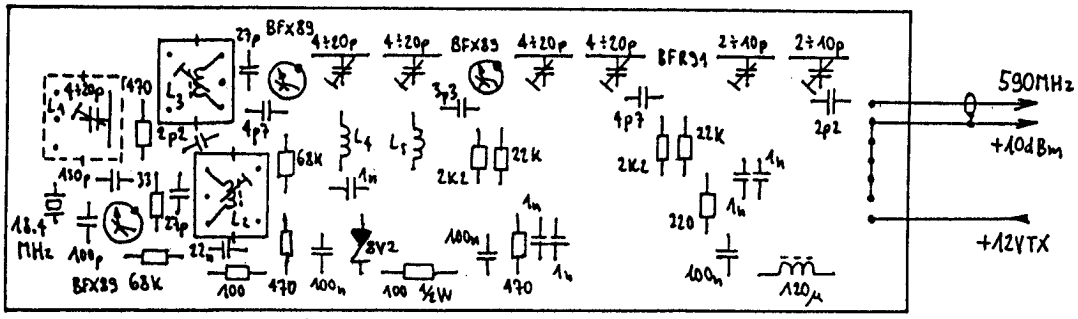


Fig. 4 - TX exciter component location.

L2 and L3 have about 150nH each or 4 turns each of 0.25mm thick copper-enameled wire. They are wound on 36MHz (TV IF) coil formers with a central adjustable ferrite screw, plastic cap and 10mmX10mm square shield. L4 and L5 are self-supporting coils with 4 turns each of 1mm thick copper-enameled wire, wound on an internal diameter of 4mm. Finally, L6, L7, L8 and L9 are etched on the

PCB.

The transmitter exciter is simply tuned for the maximum output power. The individual stages are tuned to obtain the maximum drop of the DC voltage on the base of the next-stage transistor. Of course, the base voltage has to be measured through a RF choke. The base voltage may become negative, but should not exceed -1V. Finally, the crystal oscillator is tuned to the desired frequency with the corresponding capacitive trimmer (or L1).

4. 2360MHz PSK modulator

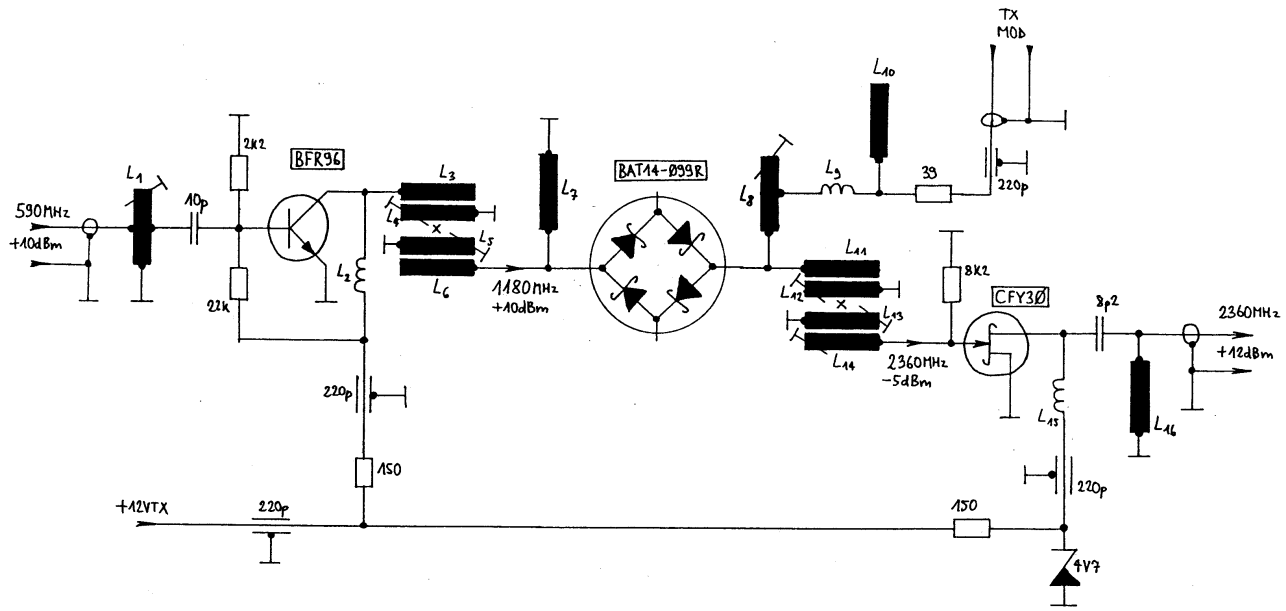


Fig. 5 - PSK modulator circuit diagram.

The circuit diagram of the 2360MHz PSK modulator is shown on Fig.5. Except for the modulator (balanced mixer) itself, the module includes the last frequency-doubler stage, bandpass filters for 590MHz, 1180MHz and 2360MHz and an output amplifier stage to boost the signal level to about 15mW. All of the filters and other frequency-selective components are made as microstrip resonators on a 1.6mm thick glassfiber-epoxy laminate FR4.

The input resonator (L1) functions as an open circuit for the input frequency (590MHz) and as a short circuit for the output frequency (1180MHz) of the frequency doubler. In this way the operation of the doubler is less sensitive to the exact cable length and output impedance of the exciter. The output bandpass (L3, L4, L5 and L6) should not only suppress the input frequency (590MHz) but also its fourth harmonic (2360MHz) that could disturb the symmetry of the balanced mixer resulting in an unsymmetrical, distorted PSK.

A harmonic mixer with anti-parallel diodes is used as the PSK modulator, since this circuit provides a reasonable unwanted carrier suppression (25dB) without any special tuning and without access to expensive test equipment (spectrum analyzer). The harmonic mixer uses a quad schottky diode BAT14-099R, since four diodes provide a higher output signal level than just two anti-parallel diodes.

The mixer is followed by a bandpass filter for 2360MHz (L11, L12, L13 and L14) to remove the 1180MHz driving signal and other unwanted mixing products far away from the 13cm frequency band. The generated PSK signal at 2360MHz does not require any filtering itself. Since the 2360MHz signal level is low, about 0.3mW, a GaAs FET amplifier stage (CFY30) is used to raise the signal level to about 15mW.

Fig. 6 - PSK modulator PCB (double-sided 1.6 mm glassfiber-epoxy, microstrip circuit with a continuous groundplane).

The PSK modulator is built on a double-sided PCB with the dimensions of 40mmX120mm. Only the upper side is shown on Fig.6, since the lower side functions as the micro-strip ground-plane and is not etched. The PCB is made of 1.6mm thick glass-fiber-epoxy laminate FR4, although this material has substantial RF losses at 2.36GHz. The component location of the PSK modulator is shown on Fig.7 for both sides of the PCB.

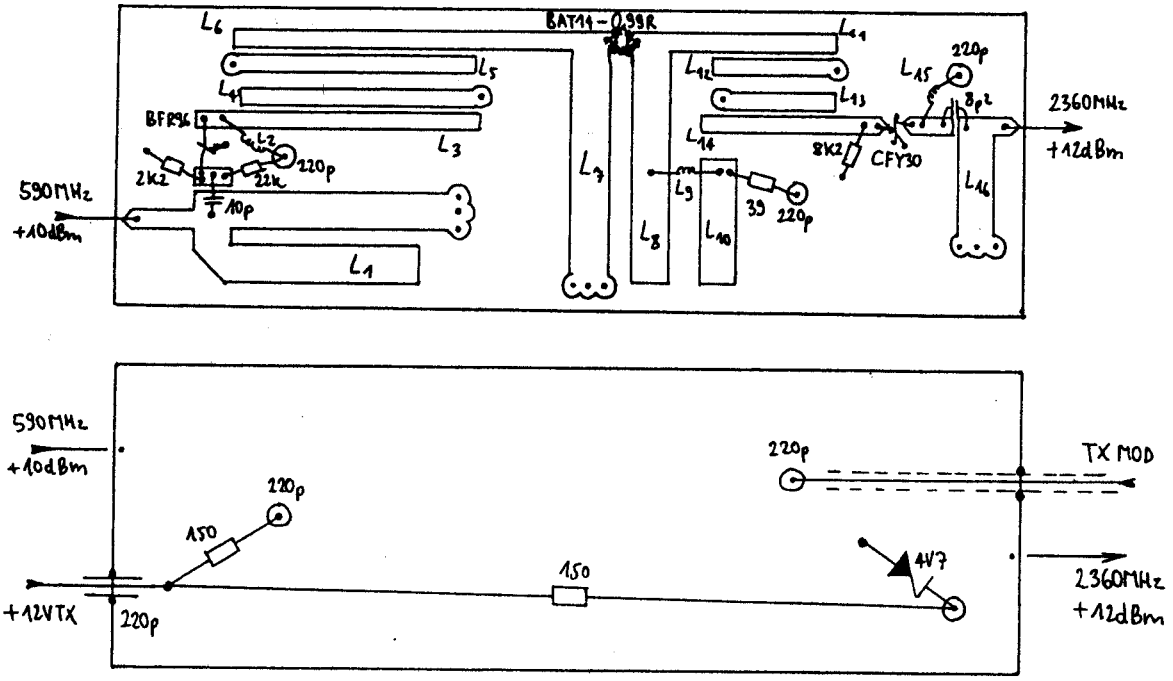


Fig. 7. - PSK modulator component location.

Although most of the transmission lines are etched on the PCB, L2, L9 and L15 are air-wound quarter-wavelength chokes. L2 is a quarter-wavelength choke for 1180MHz, L15 is a quarter-wavelength choke for 2360MHz while L9 should be a quarter-wavelength somewhere in the middle (around 1700MHz), since it has to be effective for both frequencies.

The described PSK modulator can simply be tuned for the maximum output signal level. Besides the 590MHz exciter signal, a digital modulating signal is required as well. The latter may be a square wave of the appropriate frequency or better the real digital packet-radio signal. Without any alignment, the PSK modulator will already provide an output of a few milliwatts. After any alignment of the micro-strip resonators one has to check the modulation signal level to find the best operating condition of the harmonic mixer.

5. 2360MHz RF front-end

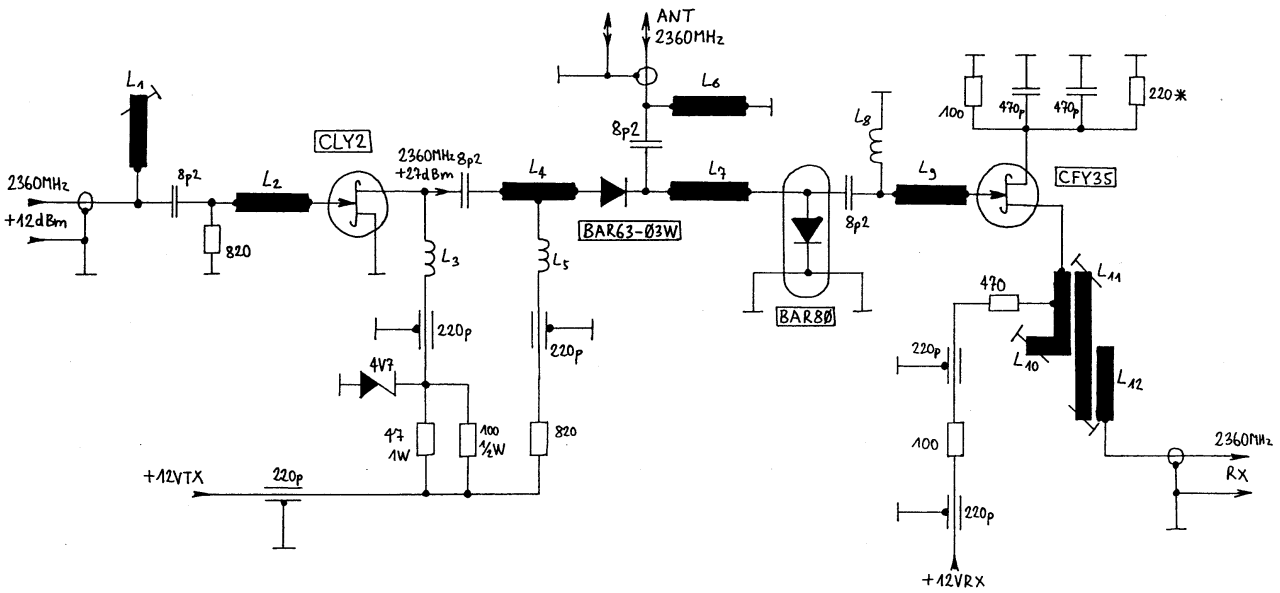


Fig. 8 – RF front-end circuit diagram.

The circuit diagram of the 2360MHz RF front-end is shown on Fig.8. The RF front-end includes the transmitter power amplifier, the receiver low-noise preamplifier and the PIN antenna switch. The RF front-end is the only module including micro-strip circuits, that is built on a low-loss, 0.8mm thick glass-fiber-teflon laminate with a dielectric constant of 2.5.

The circuit of the RF front-end is simplified by using modern SMD semiconductor devices, originally developed for cellular telephones. The transmitter power amplifier uses a single GaAs transistor CLY2 that provides both 15dB gain and more than 500mW of output power at the same time. Just a few years ago, an equivalent circuit would require three or four silicon bipolar transistors. The CLY2 is a low-voltage power GaAs FET that operates at a drain voltage of just 4.5V, while generating its own negative gate bias voltage by rectifying the input RF signal.

The antenna switch includes two different PIN diodes: BAR63-03W and BAR80. The semiconductor chips of these two diodes are similar, but there is an important difference in the packages. The BAR63-03W is built in a standard microwave SMD diode package with a low parasitic capacitance and is used as a series switch. On the other hand, the BAR80 diode is built in a low parasitic inductance package and is used as a shunt switch. Both diodes are turned on while transmitting. The quarter-wavelength line L7 transforms the BAR80 short circuit into an open circuit for the transmitter.

The RF front-end also includes a low-noise receiving preamplifier to improve the sensitivity and image rejection of the receiver. The low-noise preamp uses a CFY35 transistor, followed by a bandpass filter. The preamplifier provides a gain of about 11dB including the antenna switch and output filter losses. The bandpass filter is required to attenuate the image response around 2210MHz.

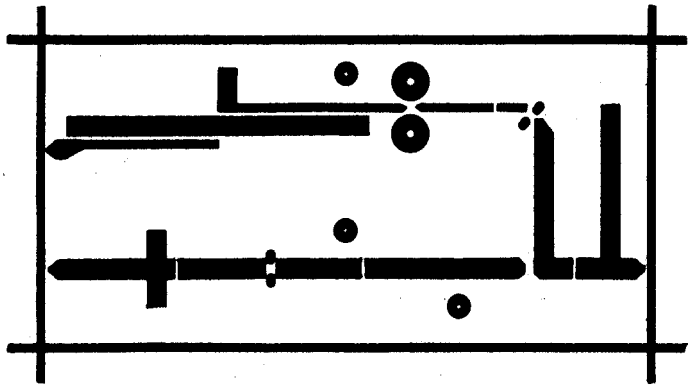


Fig. 9 - RF front-end PCB (double-sided 0.8mm glassfiber-teflon, microstrip circuit with a continuous ground plane).

The RF front-end is built on a double-sided teflon PCB with the dimensions of 40mmX80mm. Only the upper side is shown on Fig.9, since the lower side functions as the micro-strip ground-plane and is not etched. The PCB is made of 0.8mm thick glass-fiber-teflon laminate with a dielectric constant of 2.5. The component location of the RF front-end is shown on Fig.10 for both sides of the PCB. Except the printed micro-strip lines, there are three air-wound quarter-wavelength chokes for 2360MHz: L3, L5 and L8.

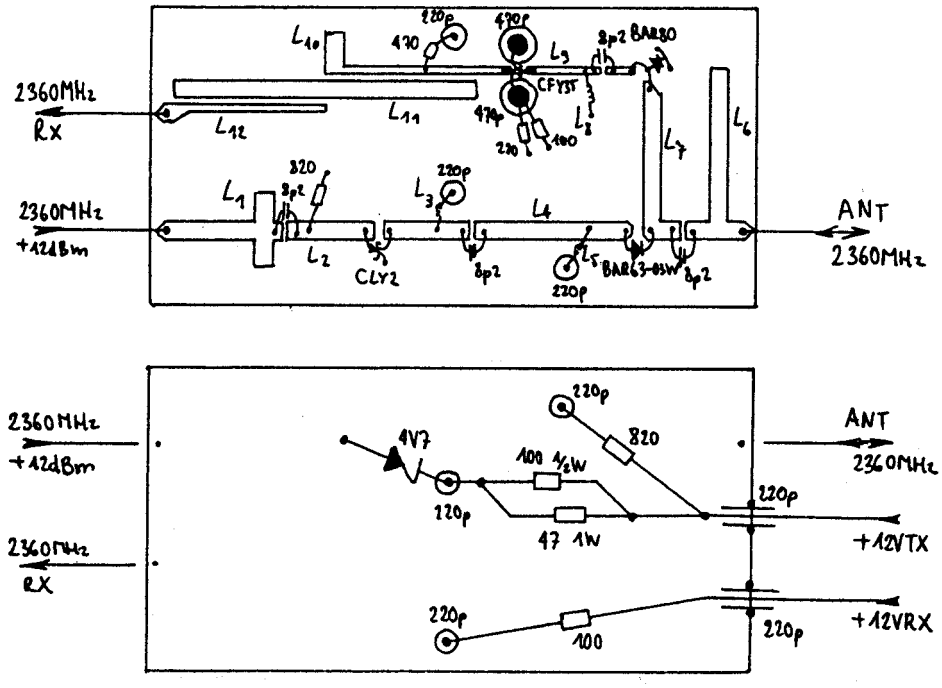
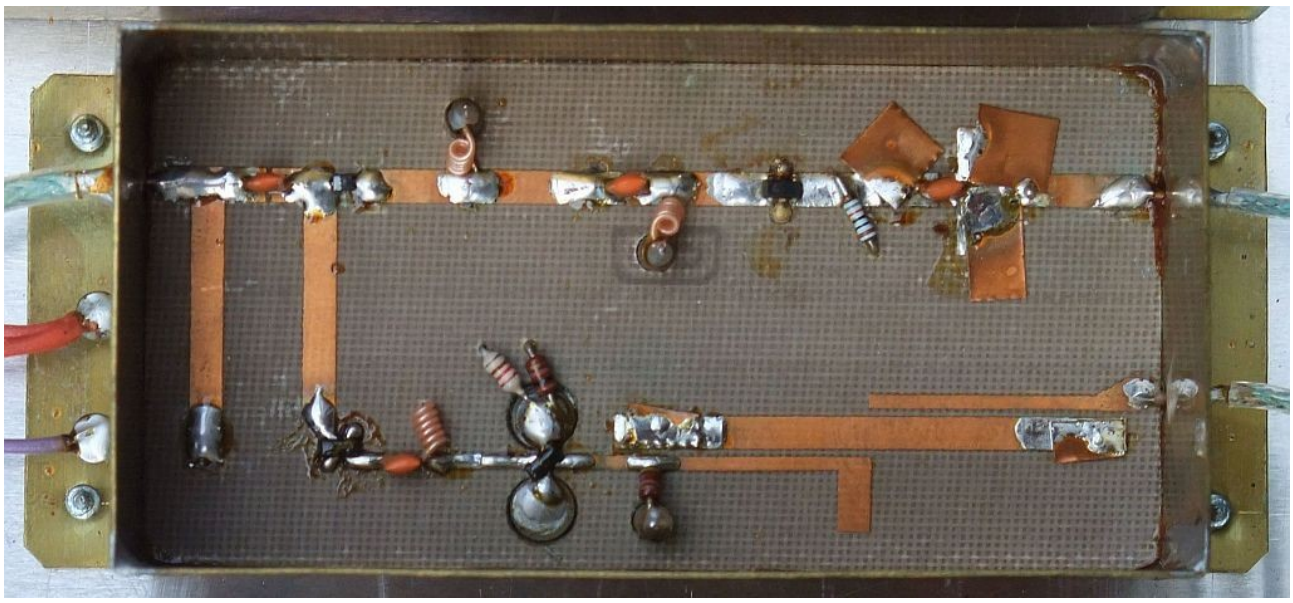


Fig. 10 - RF front-end component location.



Assembling the RF front-end, the most critical item is the correct grounding of the microwave semiconductors CLY2, BAR80 and CFY35. The CLY2 and the BAR80 are grounded through drops of solder, deposited in 2mm diameter holes at the marked positions in the teflon laminate. On the ground-plane side these holes are covered with small pieces of copper sheet that also act as heat sinks for these semiconductors. The CFY35 is grounded through two lead-less ceramic disk capacitors installed in 5.5mm diameter holes at the marked positions. The capacitors are connected to the ground-plane with small pieces of copper sheet on the other side. Finally, L6 is grounded with a 2.5mm wide strip of copper foil inserted in a slot in the teflon laminate.

The transmitter power amplifier is simply tuned for the maximum output power by adding capacity (small pieces of copper foil) to L1. Small sheets of copper foil can also be added in other parts of the circuit, but their influence is usually small when compared to L1. If the specified output power can not be obtained, the cable length between the PSK modulator and RF front-end needs to be changed.

The receiving preamplifier is also tuned for the maximum gain, but here it is more important to bring the bandpass filter to the correct frequency. The latter is adjusted with L11, while L10 only affects the CFY35 output impedance matching. Before making any RF adjustments, the DC operating point of the CFY35 has to be set by selecting appropriate source bias resistors for a Vds of 3-4V.

6. RX converter with PLL LO

To avoid several multiplier stages the receiving converter includes a microwave PLL frequency synthesizer. The converter is built as two separate modules to prevent the digital part from disturbing the low-level analog circuits. Of course each module is shielded on its own. The described RX converter is derived from a 2400MHz SSB converter published in [1].

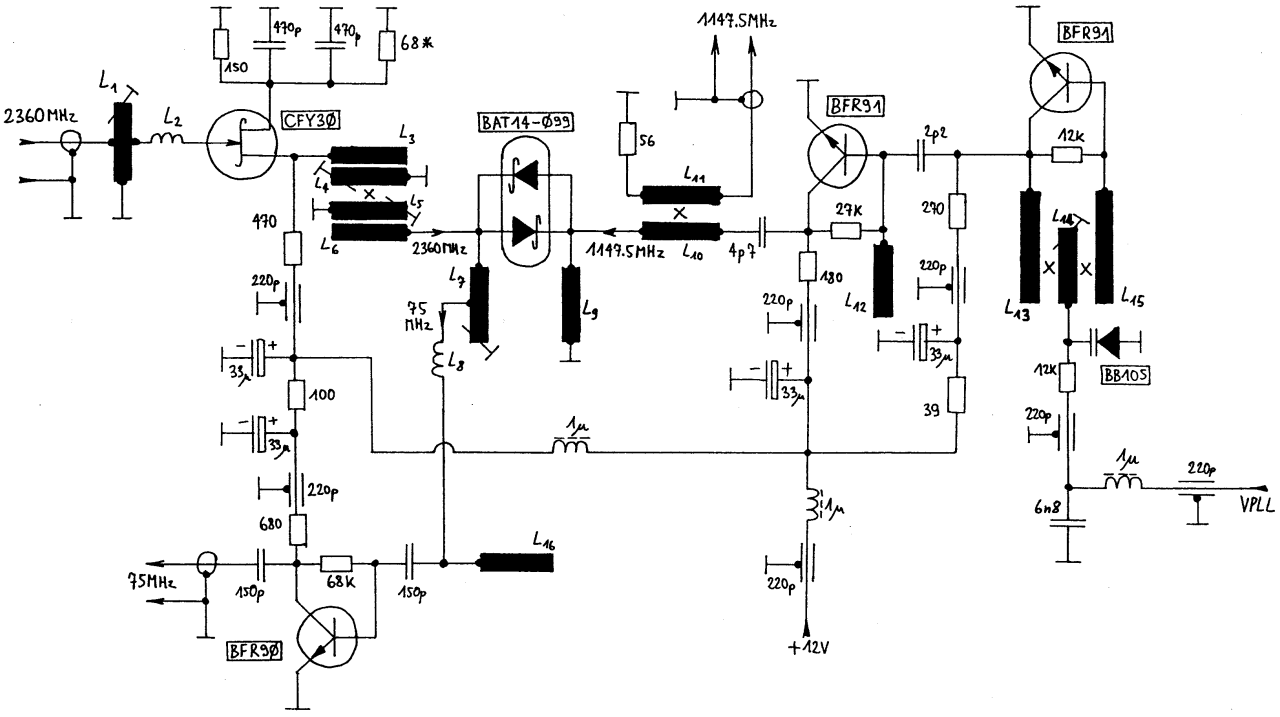


Fig. 11 – RX converter, analog section circuit diagram.

The circuit diagram of the analog section of the RX converter is shown on Fig.11. The analog section includes the second RF amplifier stage, the subharmonic mixer, the VCO including a buffer stage and the first 75MHz IF amplifier. The analog circuits are built as micro-strip circuits on a 1.6mm thick glass-fiber-epoxy laminate.

The main function of the second RF amplifier is to cover the noise figure of the harmonic mixer. The second RF amplifier is followed by another bandpass filter (L3, L4, L5 and L6), but unfortunately due to the high substrate losses this filter is unable to provide any significant rejection of the image frequency at 2210MHz. Its main purpose is to reject far-away interferences like subharmonics or even signals at the IF frequency.

The harmonic mixer uses two anti-parallel schottky diodes and is very similar to the PSK modulator. Such a mixer requires a local oscillator at half of the required conversion frequency thus simplifying the design of the PLL synthesizer. The resulting IF signal is amplified immediately to avoid any further degradation of the already poor noise figure.

The VCO uses a micro-strip bandpass filter (L13, L14 and L15) in the feedback network to obtain low phase noise. The tuning range of this VCO is thus restricted to a few percent of the central frequency. The VCO is followed by a buffer stage and part of the buffered VCO signal is coupled by L10, L11 to feed the digital section of the PLL.

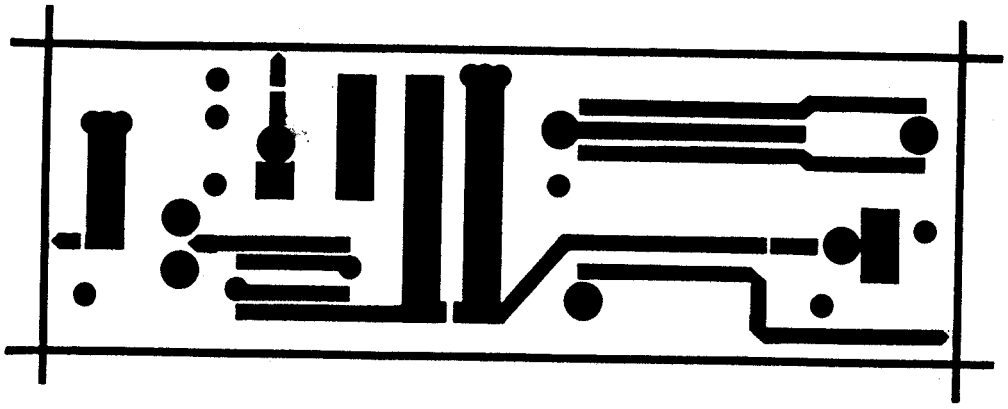


Fig. 12 – RX converter, analog section PCB (double-sided 1.6 mm glassfiber-epoxy, microstrip circuit with a continuous groundplane).

The analog section of the receiving converter is built on a double sided PCB with the dimensions of 40mmX120mm. Only the upper side is shown on Fig.12, since the lower side functions as the micro-strip ground-plane and is not etched. The PCB is made of 1.6mm thick glass-fiber-epoxy laminate FR4, although this material has substantial losses at 2.36GHz. The component location of the analog section of the RX converter is shown on Fig.13 for both sides of the PCB.

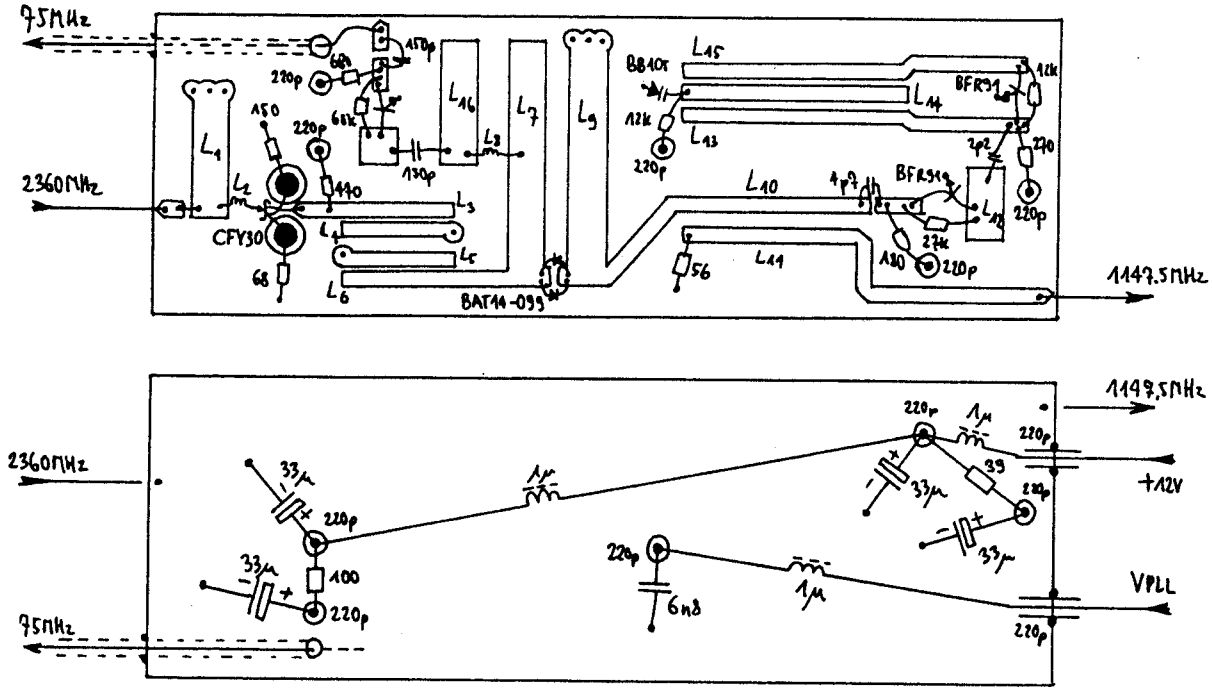


Fig. 13 – RX converter, analog section component location.

Although most of the transmission lines are etched on the PCB, there are two discrete inductors in this module. L2 is a wire loop with a 2mm internal diameter made of 0.6mm thick silver-plated copper wire. L2 may need adjustments

during the alignment of the complete transceiver. L8 is a quarter-wavelength choke around 1700MHz to be effective for both the RF and LO frequencies.

Most of the RF active devices (BFR90, BFR91 and BB105) ae installed in 6mm diameter holes in the PCB. These holes are afterwards covered on the groundplane side by soldering small pieces of copper foil. The same installation procedure also applies to the two 470pF source bypass capacitors for the CFY30 transistor. The corresponding source bias resistors are adjusted for a Vds of 3-4V.

The alignment of the analog section should start with bringing the VCO to the desired frequency range by adjusting L14. This is done easily if the PLL is already operating. L14 usually needs to be made slightly longer to obtain a 2.5V PLL control voltage in the locked condition. Then L7 is adjusted for the maximum mixer conversion gain and finally L4 and L5 may need some small adjustments. L1 and L2 should be adjusted to match the RF front-end. If the second RF stage (CFY30) is self-oscillating, the L2 wire loop has to be made shorter.

An alternative solution is to replace the CFY30 GaAs FET with the silicon MMIC INA-03184. The latter has a higher noise figure but offers more gain and does not self oscillate. When using the INA-03184, L2 has to be replaced with a 6.8pF capacitor, the output bias resistor has to be increased from 470ohm up to 680ohm and the source bypass capacitors and bias resistors are no longer required, since the two INA-03184 common pins can be grounded in a straightforward way.

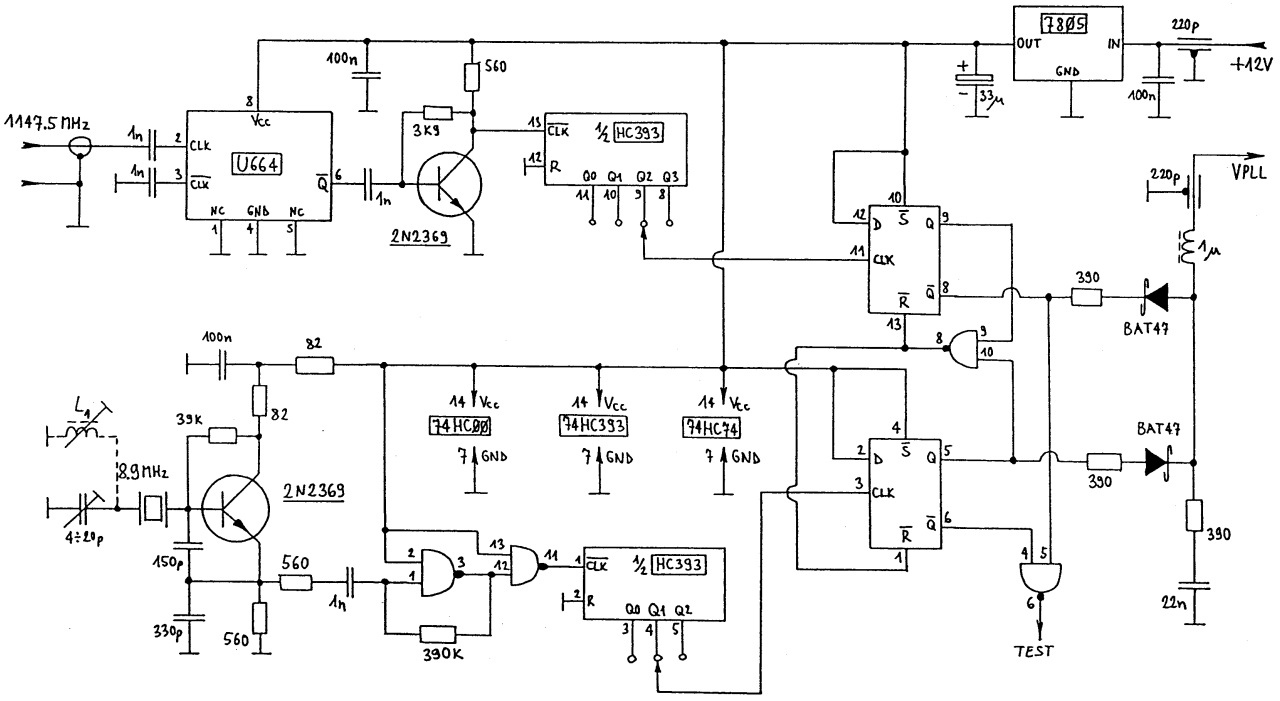


Fig. 14 – RX converter, PLL circuit diagram.

The circuit diagram of PLL section of the RX converter is shown on Fig.14. The PLL includes the /64 prescaler (U664), the reference crystal oscillator at about 8.9MHz, two additional dividers (HC393) and the frequency/phase comparator (HC74 and HC00). The PLL module has its own 5V supply voltage regulator 7805.

The above-mentioned PLL is intended to replace a chain of frequency multipliers. Therefore it does not contain variable modulo dividers. The multiplication ratio is fixed to 128 (256 when considering the harmonic mixer) and the crystal frequency has to be selected according to the desired RF channel. In the frequency range around 8.9MHz, a "CB" crystal can usually be used on its fundamental resonance. Due to the wide tolerances of CB crystals either a capacitive trimmer or a series inductor L1 may be required to bring the crystal to the desired frequency. For operation at 2360MHz, the best choice is a crystal for 26.770MHz (CB channel 22 RX).

The frequency/phase comparator drives a charge-pump output network. The correct operation of such comparators is limited to low frequencies. Therefore both the VCO and reference signals have to be divided down to about 2.2MHz when using 74HC logic in the frequency/phase comparator. Fast (schottky) diodes BAT47 are required in the charge-pump network to avoid backlash problems that seriously deteriorate the phase noise of the frequency synthesizer.

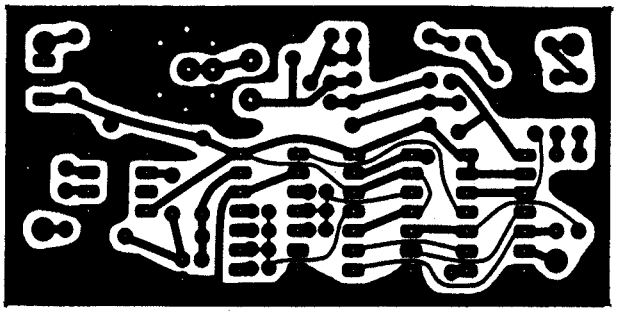


Fig. 15 - RX converter, PLL PCB (single - sided 0.8mm glassfiber - epoxy).

The PLL is built on a single-sided PCB with the dimensions of 40mmX80mm, as shown on Fig.15. The PCB is made of 0.8mm thick glass-fiber-epoxy laminate. The corresponding component location is shown on Fig.16. The only component installed below the PCB is the 1uH choke on the output.

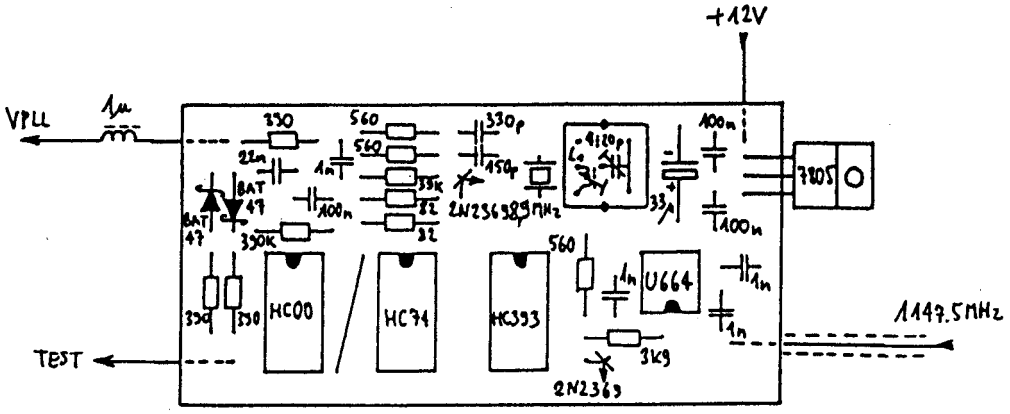
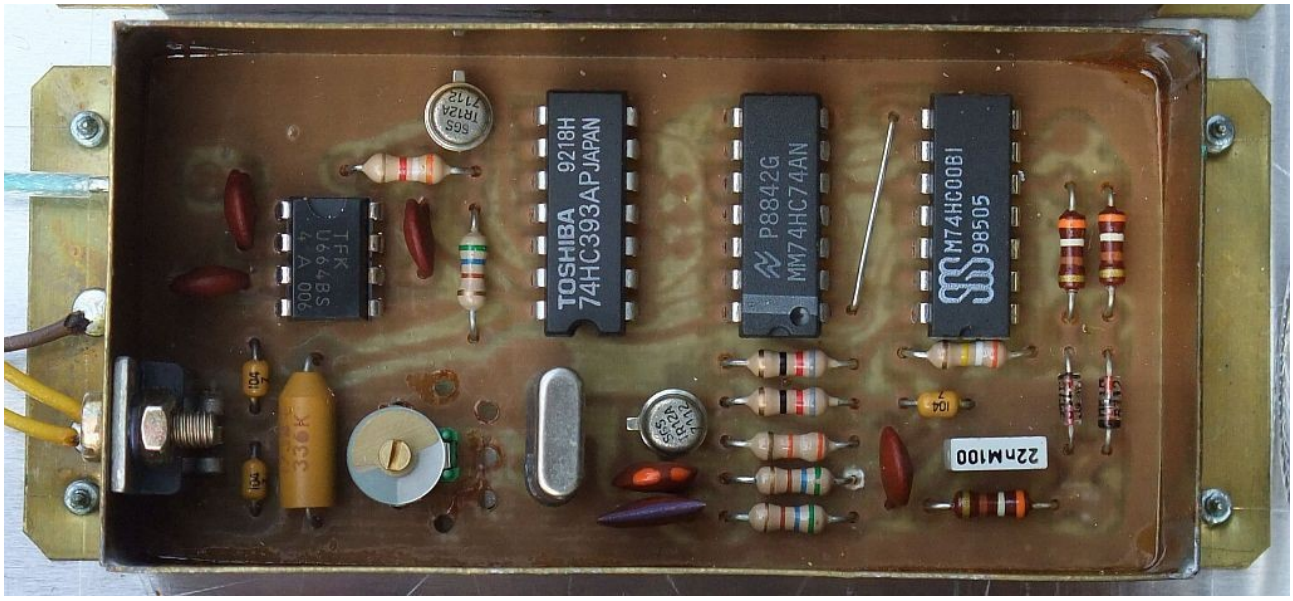


Fig. 16 - RX converter, PLL component location.



The only adjustment of the PLL is to bring the crystal oscillator to the required frequency. The PLL lock test point is not brought out of the shielding enclosure since it is only required during the adjustment of the PLL.

7. RX IF chain 75MHz/10MHz

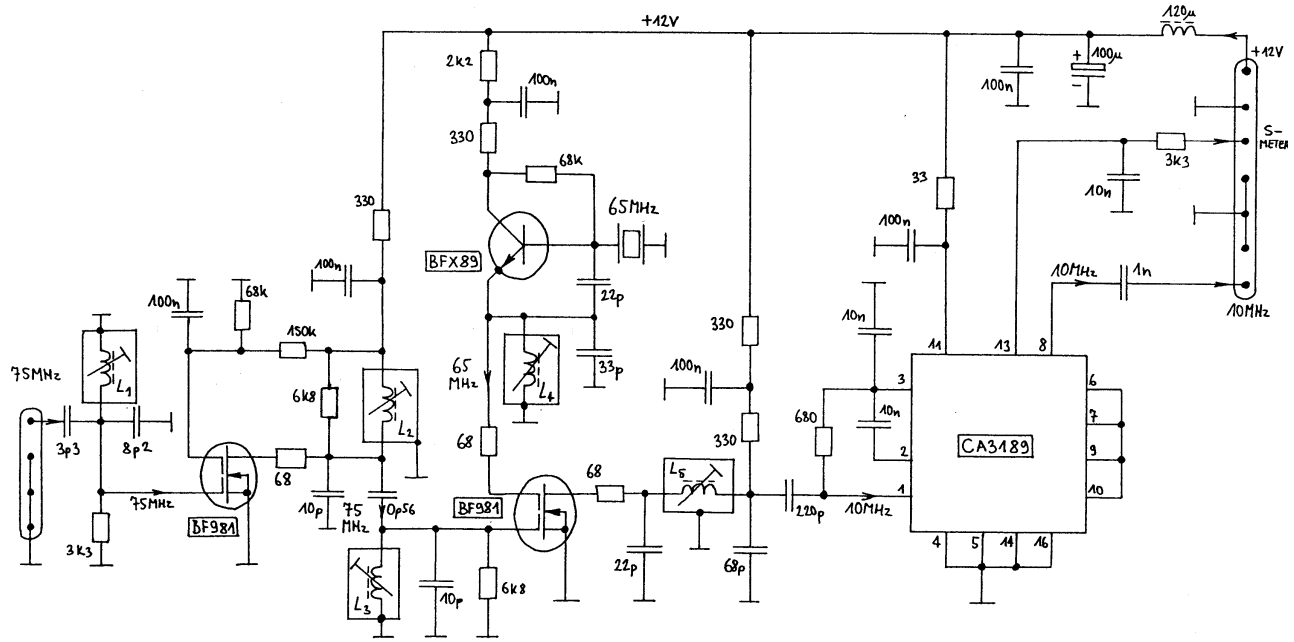


Fig. 17 - RX IF circuit diagram.

The circuit diagram of the RX IF chain is shown on Fig.17. The RX IF chain includes the second amplifier stage at 75MHz (BF981), the second mixer to 10MHz (another BF981) with its own crystal oscillator (BFX89) and the 10MHz limiting IF amplifier (CA3189).

To receive correctly the 1.2Mbit/s BPSK signal, an IF bandwidth of about 2MHz is required. Most of the receiver selectivity is provided at 75MHz, especially the two tuned circuits with L2 and L3. The contribution of the tuned circuits with L1 at 75MHz and L5 at 10MHz is smaller, since the main function of the latter is the attenuation of far-away spurious responses.

The overall IF gain is even too large, although this does not cause instability problems. The IF gain can be decreased by replacing both BF981 MOSFETs with older devices like the BF960. The second conversion oscillator uses a fifth overtone crystal at 65MHz. L4 prevents the crystal from oscillating at its fundamental resonance around 13MHz and/or at its third overtone around 39MHz.

The integrated circuit CA3189 includes a chain of amplifier stages with a high gain at 10MHz. In the described circuit, the CA3189 functions as a limiter since limiting does not distort PSK signals. Although the gain of the CA3189 drops quickly with increasing frequency, overloading the CA3189 input with the remaining 65MHz LO signal has to be prevented with the low-pass filter with L5. The CA3189 includes a S-meter output with a logarithmic response that may be very useful during receiver alignment.

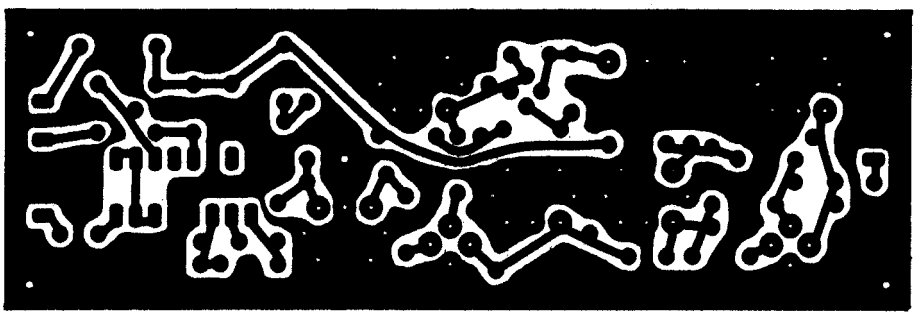


Fig. 18 - RX IF PCB (single-sided 1.6 mm glassfiber - epoxy).

The receiver IF chain is built on a single-sided PCB with the dimensions of 40mmX120mm, as shown on Fig.18. The corresponding component location is shown on Fig.19. L1, L2, L3 and L4 have about 400nH each or 5 turns of 0.15mm thick copper-enameled wire. They are wound on 36MHz (TV IF) coil-formers with a central adjustable ferrite screw, ferrite cap and 10mmX10mm square shield. L5 has about 15uH or 25 turns of 0.15mm thick copper-enameled wire. L5 is wound on a 10.7MHz IF transformer coil-former with a fixed central ferrite core, adjustable ferrite cap and 10mmX10mm square shield.

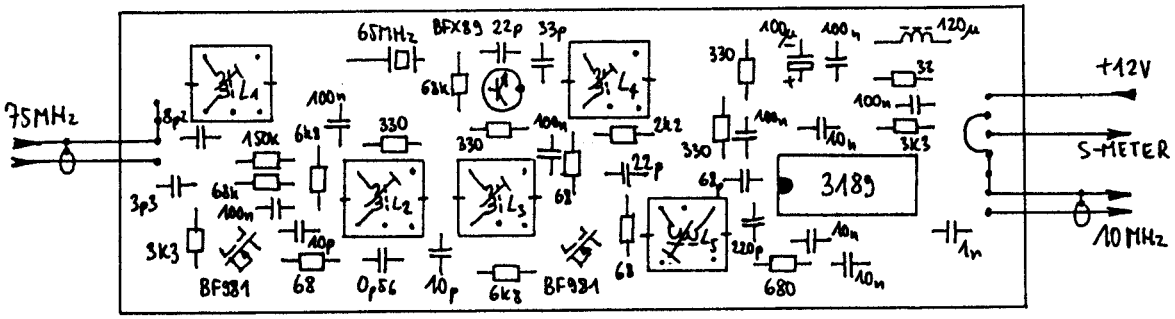


Fig. 19 - RX IF component location.

The IF chain alignment should start by checking the operation of the 65MHz crystal oscillator on the desired overtone and adjusting L4 if necessary. All other tuned circuits (L1, L2, L3 and L5) are simply aligned for the maximum gain. Since the same circuits also define the selectivity of the receiver, the alignments have to be performed using a suitable 75MHz signal source: signal generator or grid-dip meter. The receiver thermal noise or other noise sources can not be used for this purpose.

8. 1.2Mbit/s, 10MHz PSK demodulator

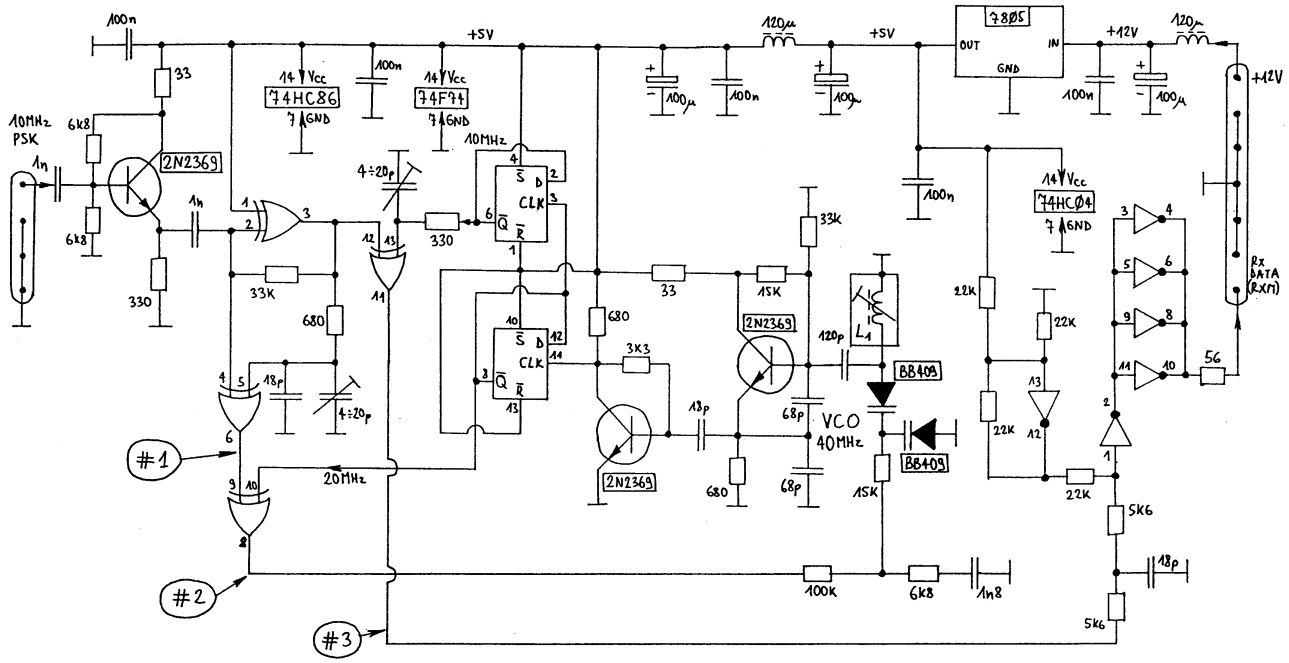


Fig. 20 - PSK demodulator circuit diagram.

Describing a PSK transceiver to radio-amateurs, the least conventional circuit is probably the PSK demodulator. There are several different possible technical solutions for a BPSK demodulator. The circuit diagram shown on Fig.20 is probably one of the simplest coherent BPSK demodulators. Its principle of operation is a squaring-loop carrier recovery, followed by a PLL filter and a mixer. EXOR gates are used elsewhere for the squaring and mixing functions.

The input 10MHz IF signal is first boosted to TTL level with an emitter follower (2N2369) followed by one of the gates of a 74HC86 (pins 1, 2 and 3). Next the IF signal is multiplied by its delayed replica (squaring or second-harmonic generation) in another EXOR gate (pins 4, 5 and 6). The delay is obtained with a RC network. On the output of this circuit, pin 6 or test point #1, a double IF carrier frequency is obtained, since the BPSK modulation is removed by the frequency-doubling operation. The latter transforms 180 degrees phase shifts into 360 degrees phase shifts or in other words a 0/180 degrees phase modulation is completely removed.

The signal available at test point #1 includes a strong spectral component at twice the carrier frequency around 20MHz, but also many spurious mixing products and lots of noise. The desired 20MHz spectral component is "cleaned" by a PLL bandpass filter, since the phase shift between the input and output signals in a PLL is well defined. A mixer is used as the phase comparator, in practice another EXOR gate (pins 8, 9 and 10). The VCO operates at 40MHz, so that a perfect square wave can be obtained at 20MHz with a simple divider by two (one half of the 74F74).

The regenerated BPSK carrier is obtained by another frequency division by two (other half of the 74F74). The BPSK demodulation is finally performed by the remaining EXOR gate (pins 11, 12 and 13 of the 74HC86). Because of the division by two, the regenerated carrier phase is ambiguous 0 or 180 degrees. As a consequence, the polarity of the demodulated data is also ambiguous and this ambiguity can not be removed in a 0/180 degrees BPSK system regardless of the type of demodulator used.

Fortunately amateur packet-radio usually uses NRZI (differential) data encoding, where level transitions represent logical zeroes and constant levels represent logical ones. The polarity of the signal is therefore unimportant and the above-mentioned drawback of 0/180 BPSK modulation does not represent a limitation in a packet-radio link. However, the polarity ambiguity has to be considered when designing data scramblers and/or randomizers for NRZI signal processing.

The PSK demodulator is followed by a RC low-pass filter to remove the carrier residuals. The low-pass is followed by an amplifier (74HC04) to boost the demodulated signal to TTL level and eventually drive a 75-ohm cable to the bit-sync unit. The PSK receiver therefore only has a digital output, there are no outputs for loudspeakers or headphones.

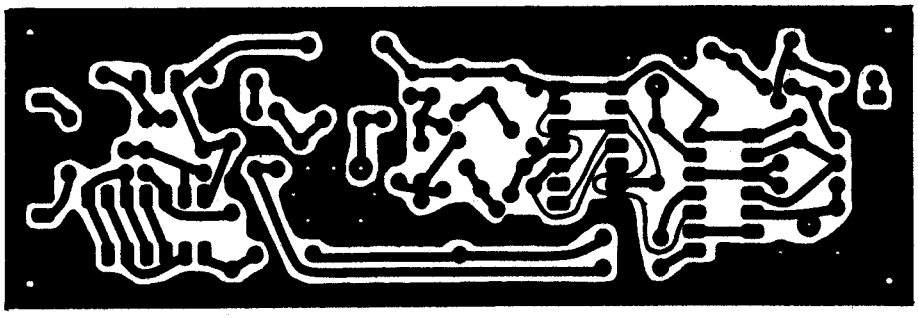


Fig. 21 - PSK demodulator PCB (single-sided 1.6mm glassfiber-epoxy).

The PSK demodulator is built on a single-sided PCB with the dimensions of 40mmX120mm, as shown on Fig.21. The corresponding component location is shown on Fig.22. The VCO components have to be selected carefully to avoid frequency drifts. The VCO capacitors must be NP0 ceramic or styroflex types with a low temperature coefficient. The VCO coil L1 has around 400nH or 6 turns of 0.15 thick copper-enameled wire on a 36MHz (TV IF) coil-former with a central, adjustable ferrite screw, plastic cap and 10mmX10mm square shield.

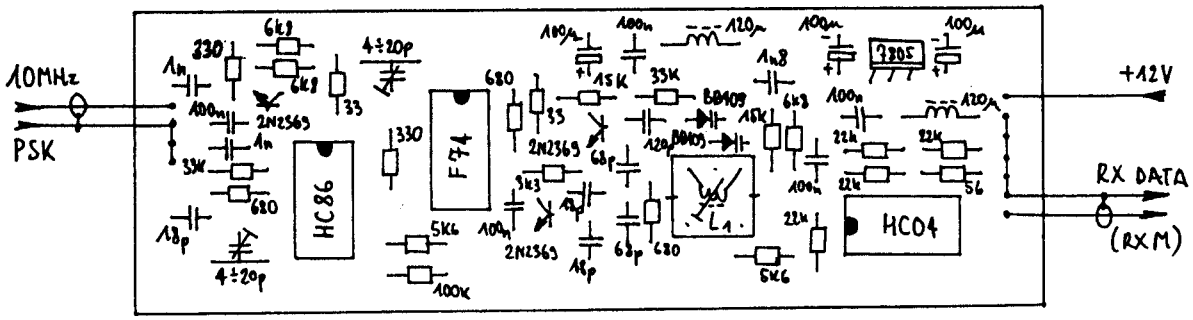


Fig. 22 - PSK demodulator component location.

The alignment of the PSK demodulator should start with the adjustment of the delay of the input signal frequency doubler. A DC voltmeter is connected to test point #1 through a RF choke. The capacitive trimmer on pin 5 of the 74HC86 is adjusted to obtain an average (DC) voltage of 2.5V on test point #1 with some input signal: either receiver noise or a valid PSK signal.

Next a coarse adjustment of L1 is performed to bring the VCO frequency to 40MHz with no input signal. Then a valid PSK signal is applied and the DC voltage on test point #2 is measured through a RF choke. The DC voltage on test point #2 should follow even small movements of the core of L1 when the PLL is locked. The core of L1 is finally adjusted for 2.5V in the locked state or in other words the DC voltage should not change when the input signal is removed and only noise is present.

Finally, the correct phase of the regenerated carrier has to be set. An oscilloscope is connected to test point #3 through a RF choke and a valid PSK signal is applied to the input. The capacitive trimmer on pin 13 of the 74HC86 is adjusted to obtain the maximum amplitude of the demodulated signal. Alternatively, a DC voltmeter can be connected to test point #3 and the PSK demodulator is driven by an un-modulated carrier. The capacitive trimmer on pin 13 is adjusted either for the maximum or minimum DC voltage, depending on the (phase ambiguity!) locking point of the PLL.

9. Supply switch interface

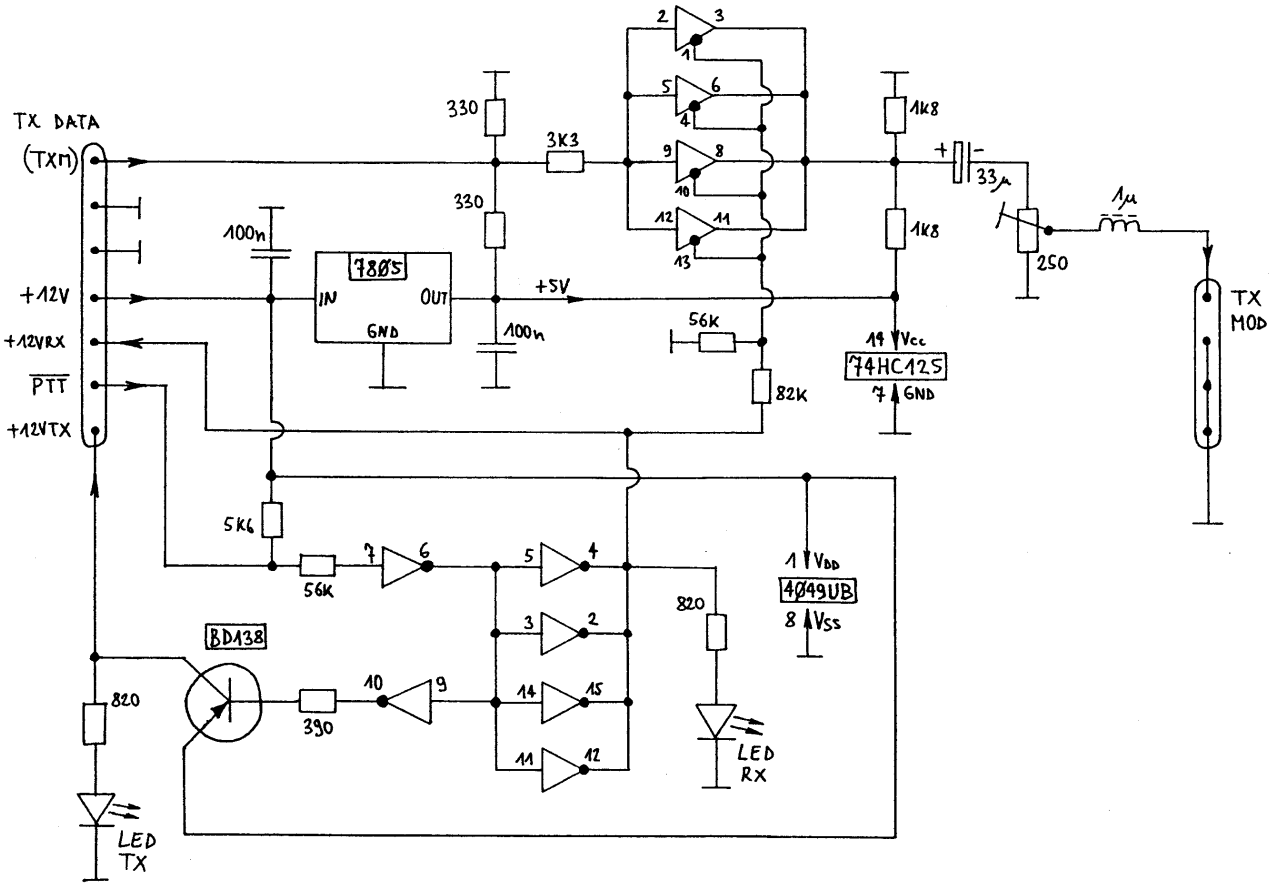


Fig. 23 - Supply switch interface circuit diagram.

The circuit diagram of the supply switch and some additional interface circuits is shown Fig.23. Most of the receiver circuits receive a continuous supply voltage of +12V. The supply switch only turns on the transmitter circuits (+12VTX) and at the same time removes the supply voltage to the RX RF preamplifier (+12VRX). The supply switching is performed by CMOS inverters (4049UB). The high TX current drain requires an additional PNP transistor BD138.

The RX/TX switching is driven by the PTT line. Just like with other transceivers, the PTT input is defined as a switch that closes towards ground when transmitting. The antenna PIN switch is driven by the +12VTX line and does not require any additional switching signals. Since most of the receiver circuits remain operational when transmitting, several of the receiver circuits (converter with PLL, PSK demodulator) can be tested with their own transmitter signal due to the inevitable crosstalk between the transmitter and the receiver.

The supply switch interface module also includes the modulator driver. The TTL input includes termination resistors to prevent cable ringing, if a longer coaxial cable is used between the transceiver and the digital equipment. The TTL input signal is first boosted by a 74HC125, followed by a resistive trimmer for the modulation level and a low-pass filter with the 1uH inductor. The modulation level is simply adjusted to obtain the maximum transmitter output power.

The 74HC125 receives the supply voltage +5V also while receiving and only its tri-state outputs are disabled during reception. The two 1.8kohm resistors keep the 33uF tantalum capacitor charged to 2.5V to speed-up the RX/TX switching. The 33uF tantalum capacitor is the only capacitive signal coupling in the whole transceiver. All other signal couplings allow the transmission of the

DC component of the digital signal. If the described PSK transceiver is to be used without a data scrambler or randomizer, the described capacitive signal coupling has to be removed by redesigning the modulator driver only, while the other circuits need not be modified.

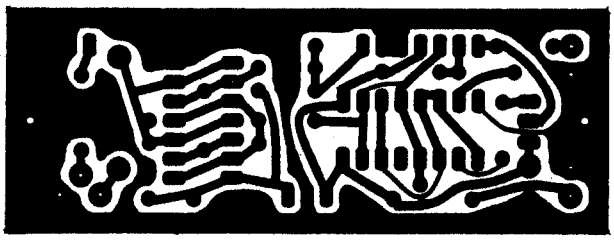


Fig. 24 - Supply switch interface PCB (single-sided 1.6 mm glassfiber - epoxy).

The supply switch interface is built on a single-sided PCB with the dimensions of 30mmX80mm, as shown on Fig.24. The corresponding component location is shown on Fig.25. The PCB is intended to be installed behind the front panel of the transceiver and is intended to carry the RX and TX LEDs.

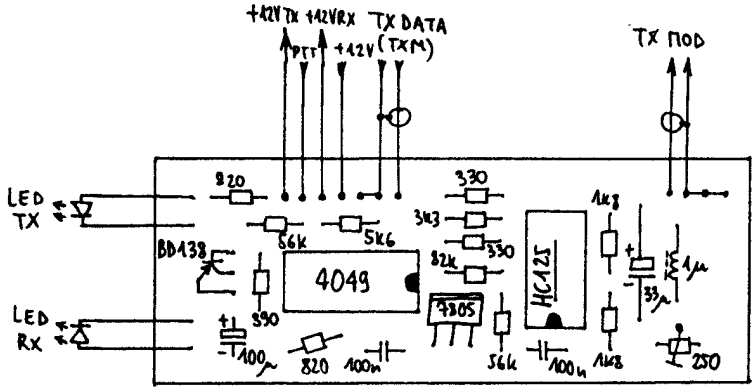
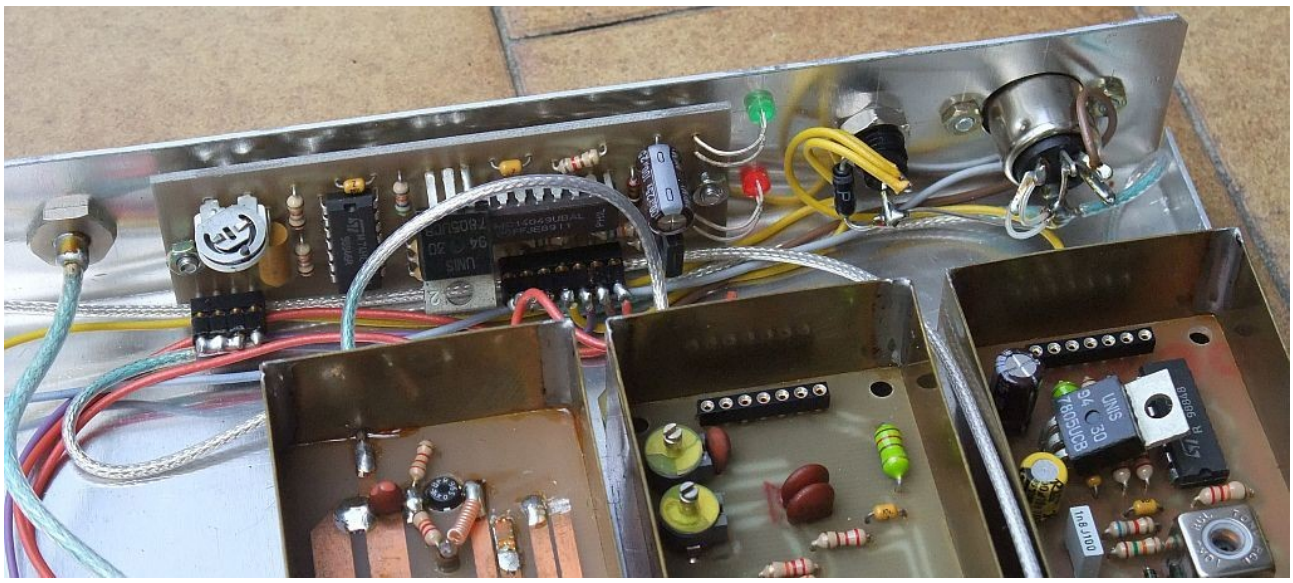


Fig. 25 - Supply switch interface component location.



10. Assembly of the 13cm PSK transceiver

Building a PSK transceiver certainly represents something new for most radio-amateurs, while the microwave frequencies make the job even more difficult. Except for the careful design of the various circuits, the mechanical layout and assembly also have to be considered right from the beginning. To avoid any possible shielding or crosstalk problems, the described transceiver employs a large number of shielded enclosures and feed-through capacitors.

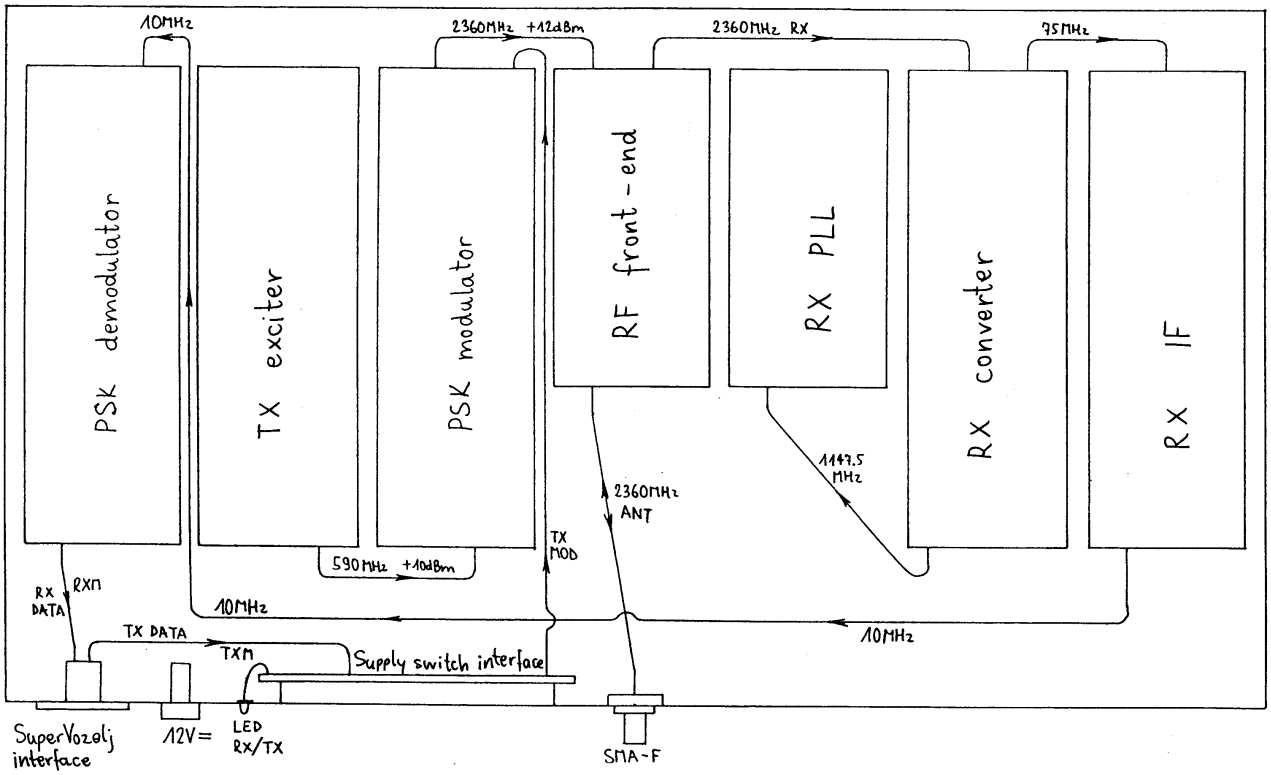
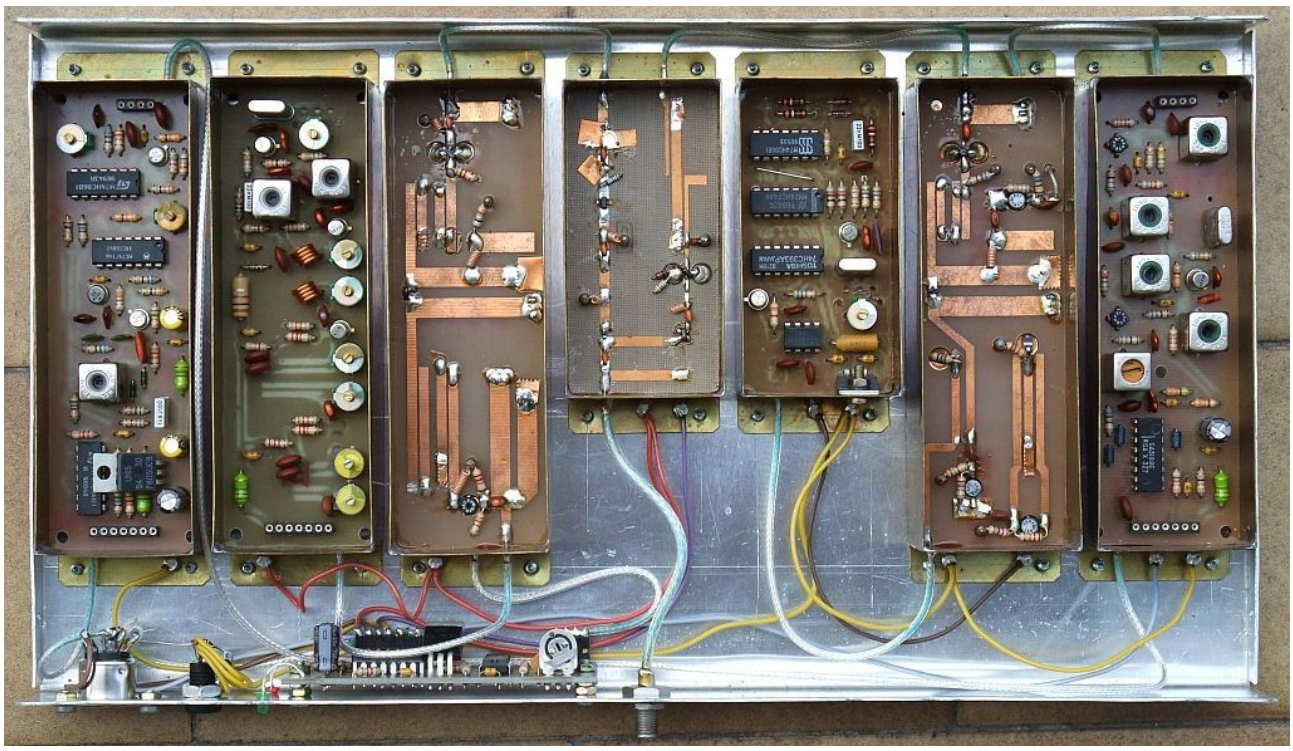
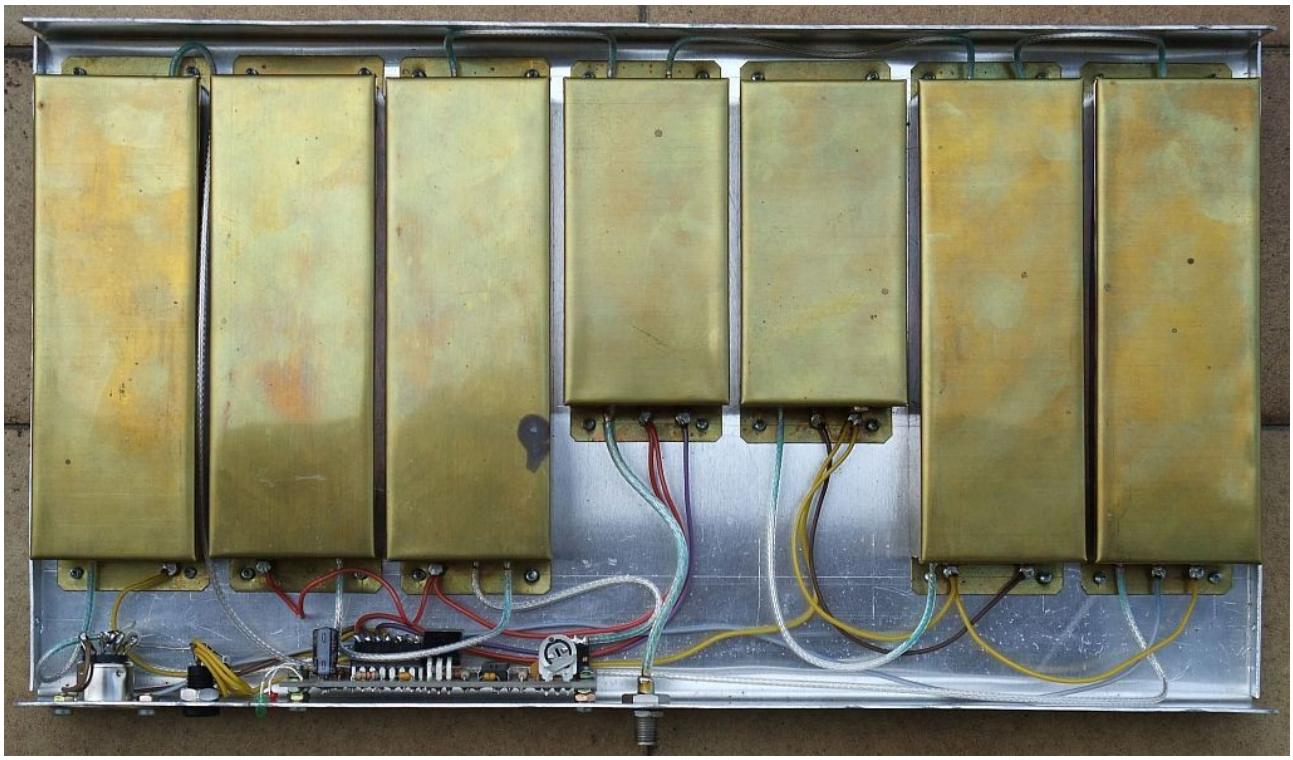


Fig. 26 - 13cm PSK transceiver module location.



The PSK transceiver is enclosed in a custom-made aluminum box measuring 320mm(width)X175mm(depth)X32mm(height). The individual module locations and RF interconnects are shown on Fig.26. The box is made of two "U"-shaped pieces of aluminum sheet. The front, bottom and back are made of 1mm thick aluminum sheet, while the cover and the two sides are made of 0.6mm thick aluminum sheet. The cover and sides are 190mm deep to exceed the size of the bottom by 7.5mm on the front and on the back.



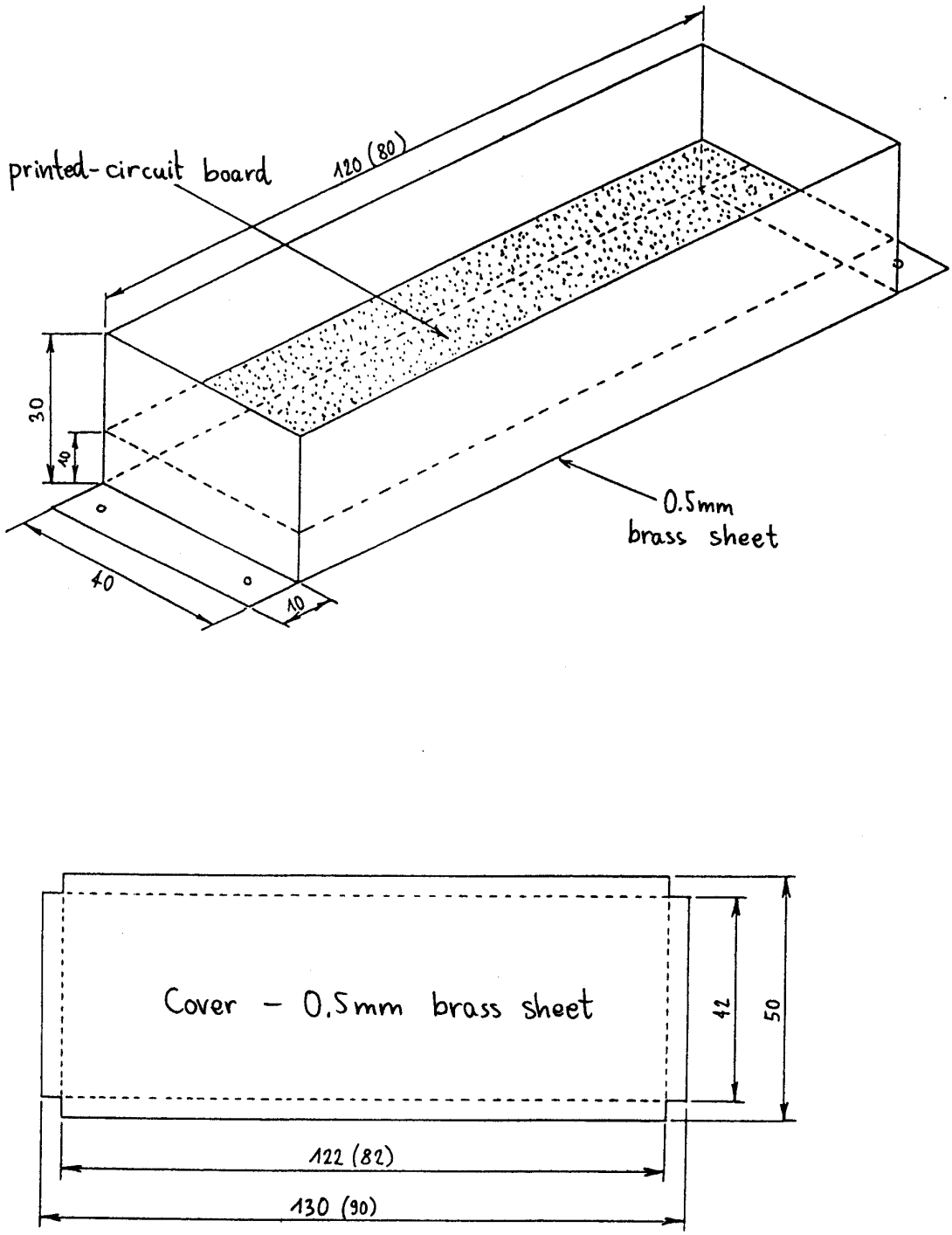
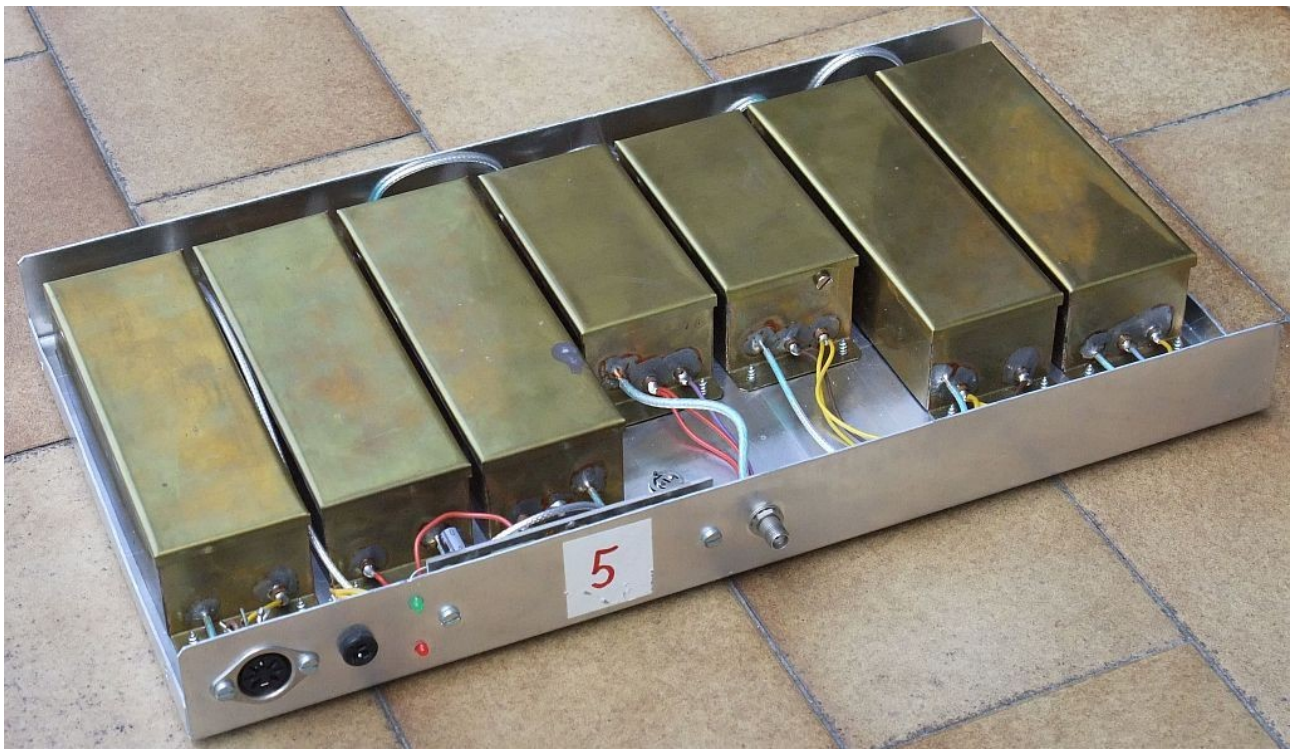


Fig. 27 – 13cm PSK transceiver shielded module enclosure.

The individual modules of the PSK transceiver are all (except the supply switch interface) installed in shielded enclosures made of 0.5mm thick brass sheet. The PCBs are soldered into a brass frame as shown on Fig.27. A brass cover is then plugged onto the frame to complete the shielding enclosure. The shielded module is then installed on the bottom of the aluminum box with four sheet-metal screws. The height of the aluminum box is selected so that the main aluminum cover keeps all seven small brass covers in position.



To retain the shielding efficiency of the single modules, all of the supply and low-frequency interconnects go through 220pF feed-through capacitors soldered in the narrow sides of the brass frames. The RF interconnects are made with thin 50-ohm teflon cables (RG-188 or similar). It is extremely important that the coax shielding braid is soldered in a "watertight" fashion to the brass sheet all around the central conductor using a suitable soldering iron.

The size and shape of the single-module shielded enclosures is selected so that the lowest waveguide mode cutoff frequency is well above the operating frequency of the transceiver in the 13cm band. The described shielded enclosures usually do not require any microwave absorbers or other countermeasures to suppress cavity resonances.

The described PSK transceiver probably represents the first serious construction using SMD parts for many amateur builders. Unfortunately SMD parts can not be avoided: at high frequencies it is essential to keep package parasitics small enough to obtain a good device gain, noise figure and/or output power. The described 13cm PSK transceiver was designed with Siemens SMD semiconductors originally intended for cellular telephones. Since these devices are relatively new, their packages and corresponding pin-outs are shown on Fig.28. Please note that due to space restrictions, the package markings are necessarily different from the device names!

11. Experimental results

The design goal of the described transceiver was to develop a packet-radio transceiver capable of transmitting data at 1Mbit/s with a free-space radio range between 500km and 1000km using moderate-size antennas. Such equipment is required for real-world line-of-sight packet-radio links of 30-100km with a single transceiver connected to more than one antenna (to support more than one link) and with a reasonable link margin of 10-15dB to counter propagation effects.

The first two transceivers were finished in April 1995 and some laboratory bit-error rate measurements were made. The acknowledges go to Knut Brenndoerfer, DF8CA, that supplied the author with up-to-date microwave SMD components. The first packet-radio link was installed in June 1995 between the SuperVozelj packet-radio node GORICA:S55YNG and the experimental node RAFUT:S59DAY at the author's QTH.

Although the distance is only 5.8km, there is no optical visibility between these two locations. The obstacle (hill) exceeds the 10th Fresnel zone at 13cm and the reception of a commercial UHF TV repeater installed in the same location is not possible due to reflections corrupting the horizontal sync pulses. Nevertheless, two-way packet-radio communication at 1.2288Mbit/s was found possible although affected by fading, using the described 13cm PSK transceivers, 16dBi short-backfire (SBF) antennas and about 5dB of antenna cable loss at each side of the link!

The first operational 1.2288Mbit/s packet-radio link was installed at the end of July 1995 between the SuperVozelj packet-radio nodes GORICA:S55YNG and KUK:S55YKK at a distance of 22.1km. Next this link was extended to the SuperVozelj node IDRIJA:S55YID in the beginning of October 1995, at a distance of 36.6km from KUK:S55YKK. The measured YKK-YID link margin is 17dB, although there are two SBF antennas at KUK:S55YKK pointed in different directions, but connected to one single 13cm PSK transceiver. The estimated cable losses are around 3dB at each side of the link.

All of these experiments are using SuperVozelj node computers [2]. The SuperVozelj packet-radio node computer is based on the MC68010 16-bit CPU and offers 6 low-speed interrupt-serviced channels up to 76.8kbit/s for user access (three Z8530 SCC chips) and two high-speed DMA-serviced channels for megabit interlinks (Z8530 SCC + MC68450 DMA). The interface to the described 13cm PSK transceiver includes external bit-sync/clock recovery and a 1+X**12+X**17 polynomial data scrambler/randomizer.

Currently seven prototypes of the described 13cm PSK transceiver have been built and four are already installed on mountaintop digipeaters. Together these prototypes accumulated more than one year of continuous operation with no failures. However, the described transceivers have not been checked in winter conditions yet, under wider temperature excursions to lower temperatures.
The described 13cm PSK transceivers finally demonstrated that megabit amateur packet-radio is not just possible but it is also a practical alternative. Using more sophisticated PSK transceivers with a larger radio range, a single PSK transceiver can be connected to more than one antenna and thus replace many narrowband FM "interlink" transceivers resulting in a simpler and cheaper packet-radio network. Of course, the next logical step is to develop simpler PSK transceivers for the user community, maybe using direct-conversion PSK demodulation.

12. References

[1] Matjaž Vidmar, S53MV: "Ein Front-End fuer den Satellitenempfang im 13-cm-Band", AMSAT-DL Journal 2-94, pages 21-33.

[2] Matjaž Vidmar, S53MV: "1.2Mbit/s SuperVozelj packet-radio node system", 40. Weinheimer UKW-Tagung, 16./17. September 1995, Scriptum der Vortraege, pages 240-252.

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